Computer Evolution over the Next Decade: Fact or Fiction?

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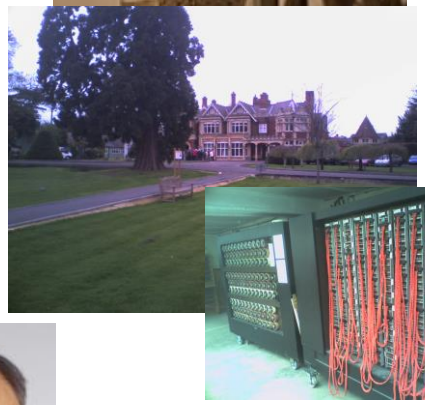
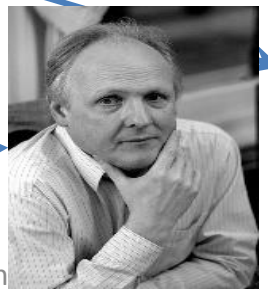
UK & Ireland Chapter
IEEE Computer Society

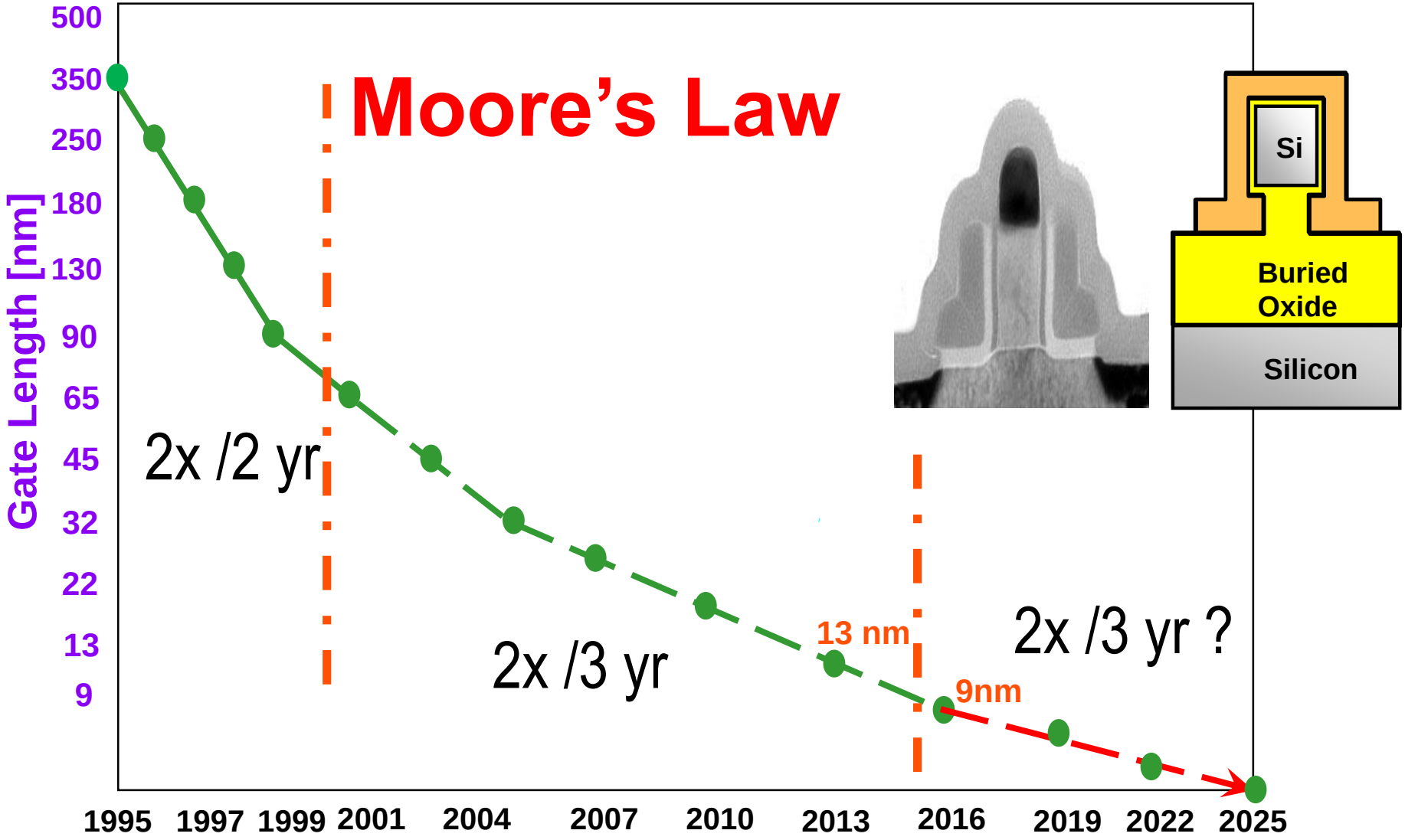
Computing Laboratory, Kent

An Evolutionary History of Computer Science

1822 Charles Babbage
1937 Iowa State University
1939 Alan Turing
1943 ENIAC
1953 COBOL
1958 Integrated circuit
1964 Mouse/GUI
1971 Floppy disk
1971 Memristor by Leon Chua
1973 Ethernet
1974 IBM PC
1976 Apple
1985 MS Windows
1990 WWW by Tim Berners-Lee
1999 Wi-Fi
2004 Firefox
2008 HP Memristor
2010 iPad
2012 Memristors: Brain-like computer
2014 SpiNNaker (BCS Lovelace Medal)
2025 Future Computers???







Computers evolve fast and the processing power/integration density should double every two years by Moore's Law. In 2005, Moore said that as transistors reach the atomic scale we may encounter fundamental barrier we can't cross.

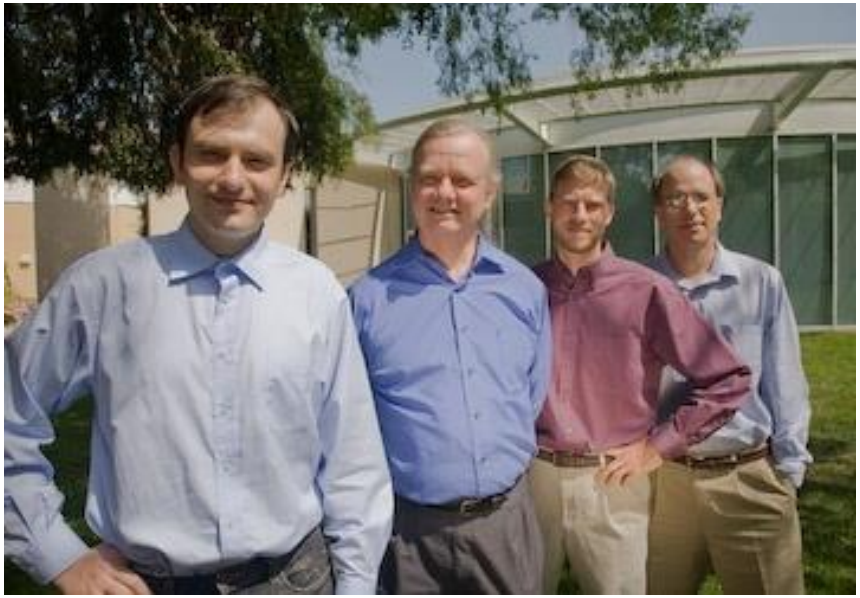
1. Brain-like Computer
2. Green Computing
3. Cloud Computing/Big Data

Memristors

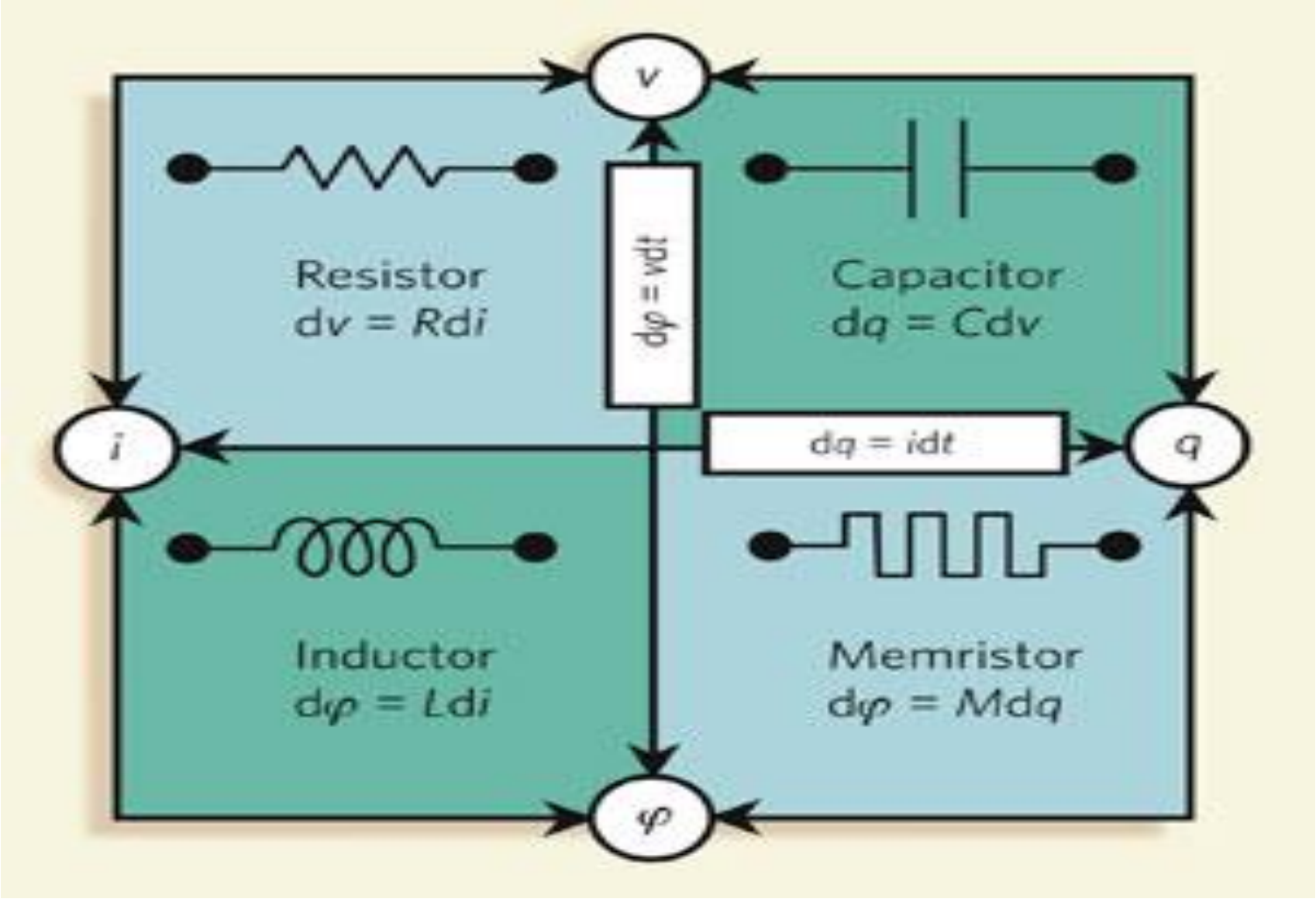
- In 1971 Prof Chua defined the memristor conceptually and mathematically.

The Memristor: Missing Circuit Element Found

- In May 2008, Dr Stan Williams and his team from HP Labs published a paper in Nature “The Memristor: Missing Circuit Element Found”



What is a Memristor



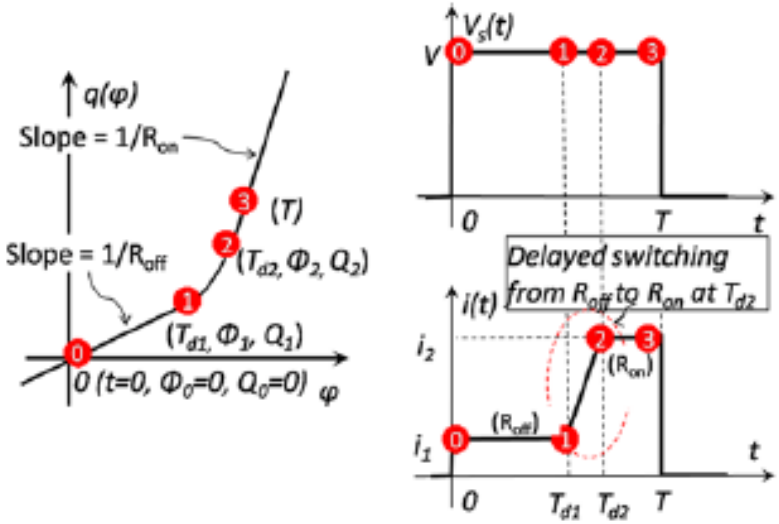
IEEE ELECTRON DEVICE LETTERS Volume 31, Issue 7, 2010 1

Delayed Switching in Memristors and Memristive Systems

Frank Zhigang Wang, *Senior Member, IEEE*, Na Helian, Sining Wu, Mian-Guan Lim, Yike Guo, and Michael Andrew Parker

***Abstract*—It was found that the switching in a memristor takes place with a time delay (this peculiar feature is named "the delayed switching"). This feature has been verified by a circuit-based experiment. The physical interpretation of this phenomenon is that an electron element possesses certain inertia, i.e., charge q or flux φ is inertial with the tendency to remain unchanged (settle to some equilibrium state). It cannot respond as rapidly as the fast variation in the excitation waveform and always takes a finite but small time interval to change its resistance value, as it must take place in a memristor or memristive system. In addition, a potential application of using this feature in ultradense computer memory has been discussed.**

***Index Terms*—Electronic device, memristive system, memristor, random access memory, resistively switching.**



(a) Piecewise linear ϕ-q; (b) Full selection as an example

JOURNAL OF APPLIED PHYSICS **111**, 000000 (2012)

Delayed switching applied to memristor neural networks

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[1]*Future Computing Group, School of Computing, University of Kent, United Kingdom*
[2]*School of Computer Science, University of Hertfordshire, United Kingdom*
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[4]*CERN, Geneva, Switzerland*

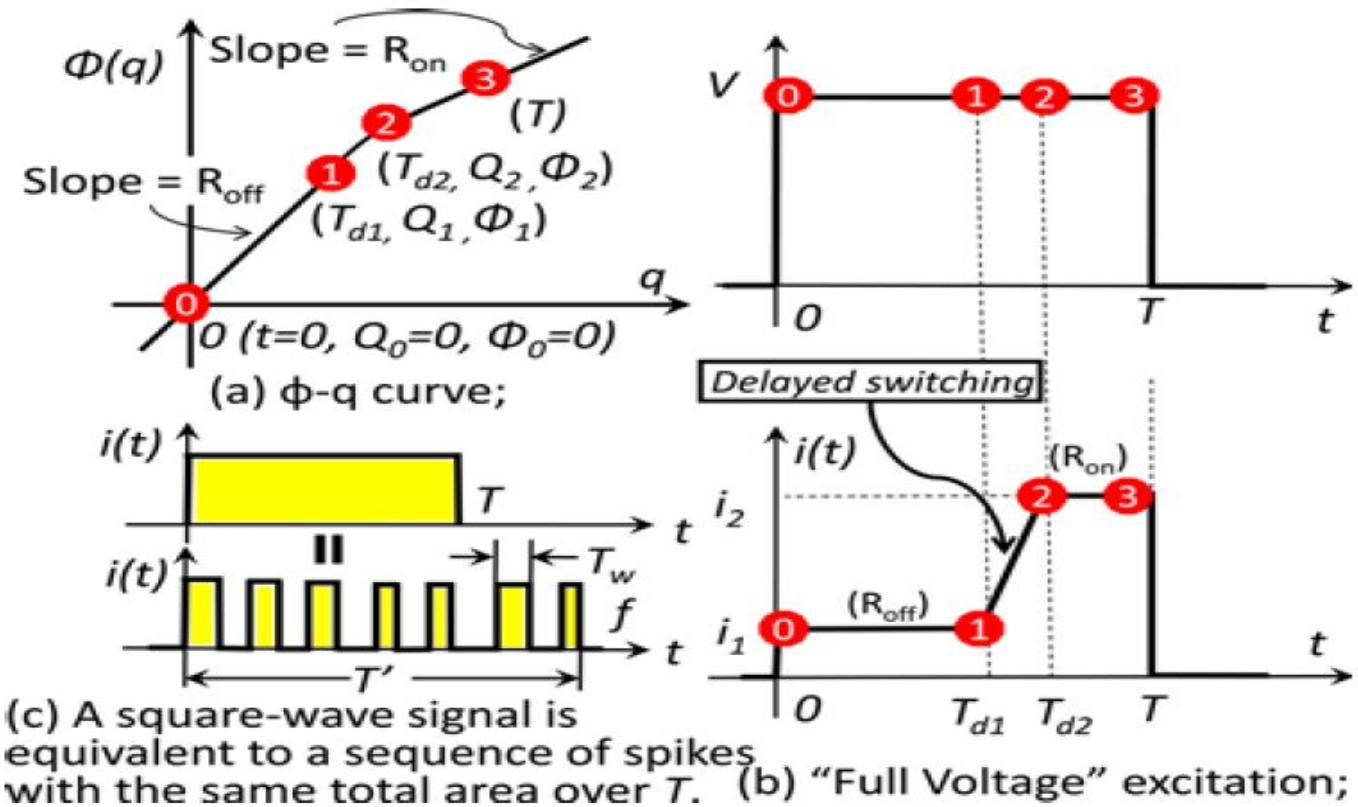
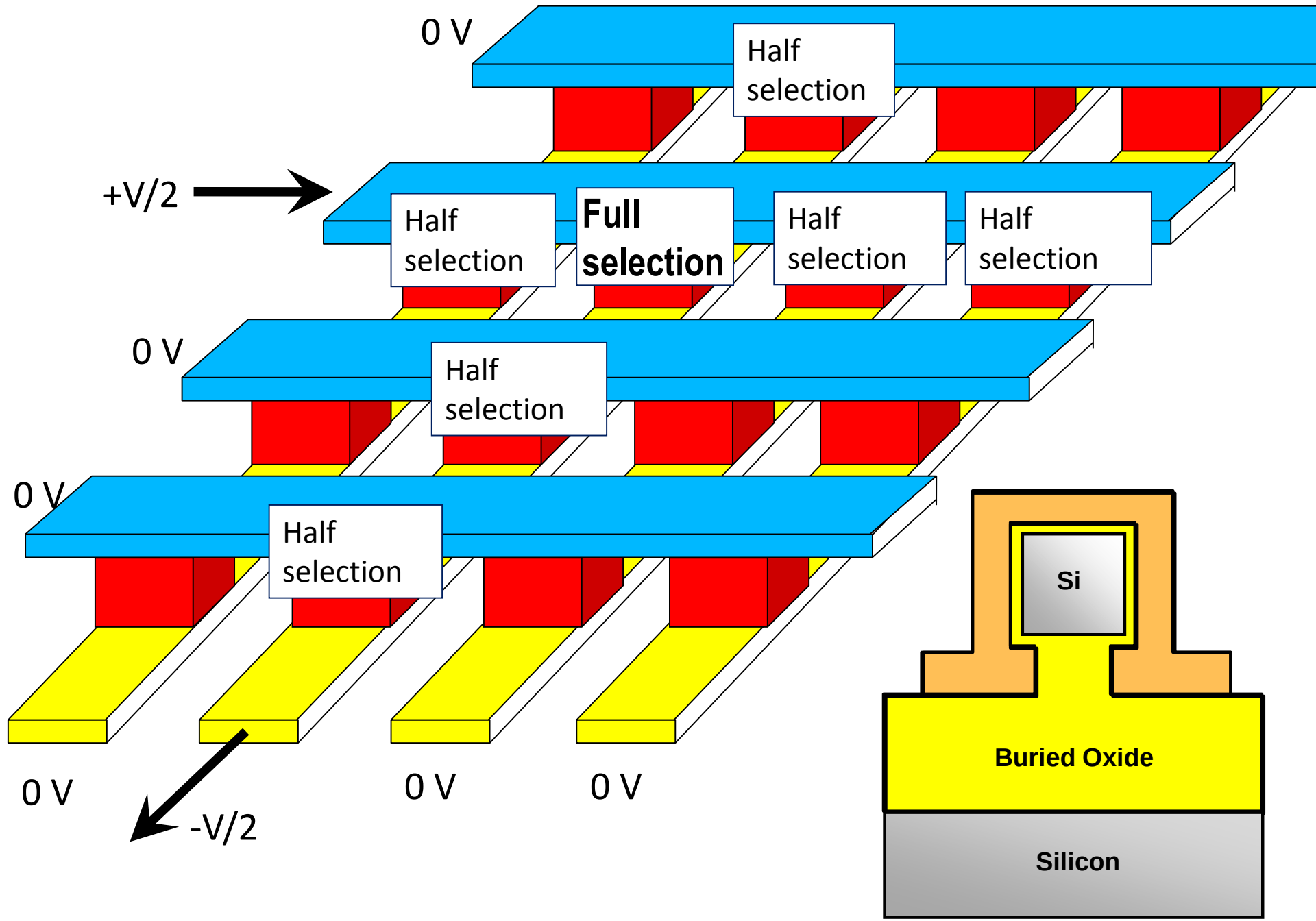


FIG. 1. (Color online) Memristor's delayed switching effect (Refs. 3 and 4): the switching from one resistance state to another due to an input voltage pulse takes place with a time delay. The effect also applies to a sequence of spikes, well used in neural networks.



Brain-like computers

- A neuron connects 20,000 synapses.
- Four orders of magnitude
- 2-terminal element
- A nanometer Cambridge junction

PRL **103,** 166802 (2009) PHYSICAL REVIEW LETTERS week ending 16 OCTOBER

Charge Confinement and Doping at $LaAlO_3/SrTiO_3$ Interfaces

T. Fix, F. Schoofs, J. L. MacManus-Driscoll, and M. G. Blamire

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(Received 29 June 2009; published 16 October 2009)

The thickness and origin of the free charge layer which forms at the $LaAlO_3/SrTiO_3$ interface is still uncertain. By inserting Mn dopants at different distances from the interface we can locate the position of carriers within the $SrTiO_3$ surface layers. We show that the majo
samples are confined within 1 unit cell of the interface. This confir
proposed for this system but the low mobility of these carriers
materials for applications and a more complete understanding
mobility carriers identified.

DOI: 10.1103/PhysRevLett.103.166802 PA

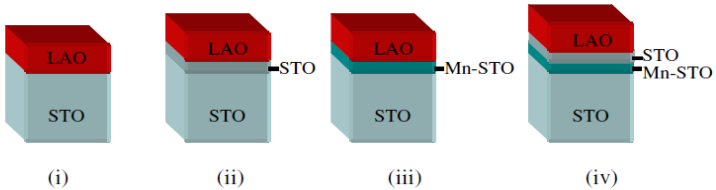
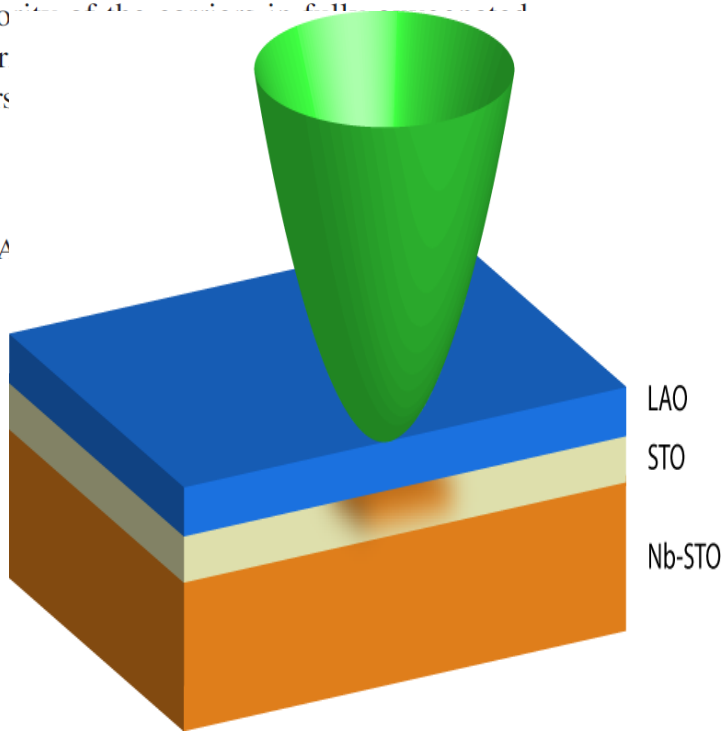
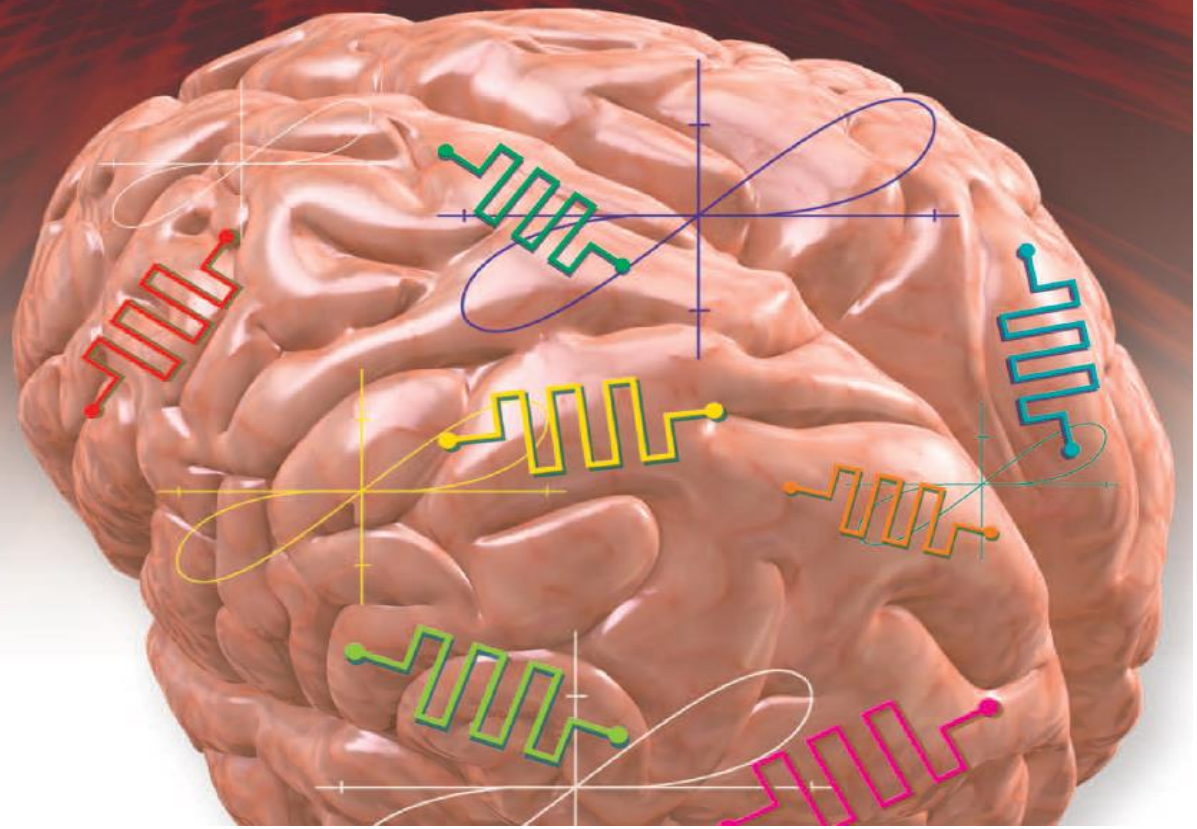


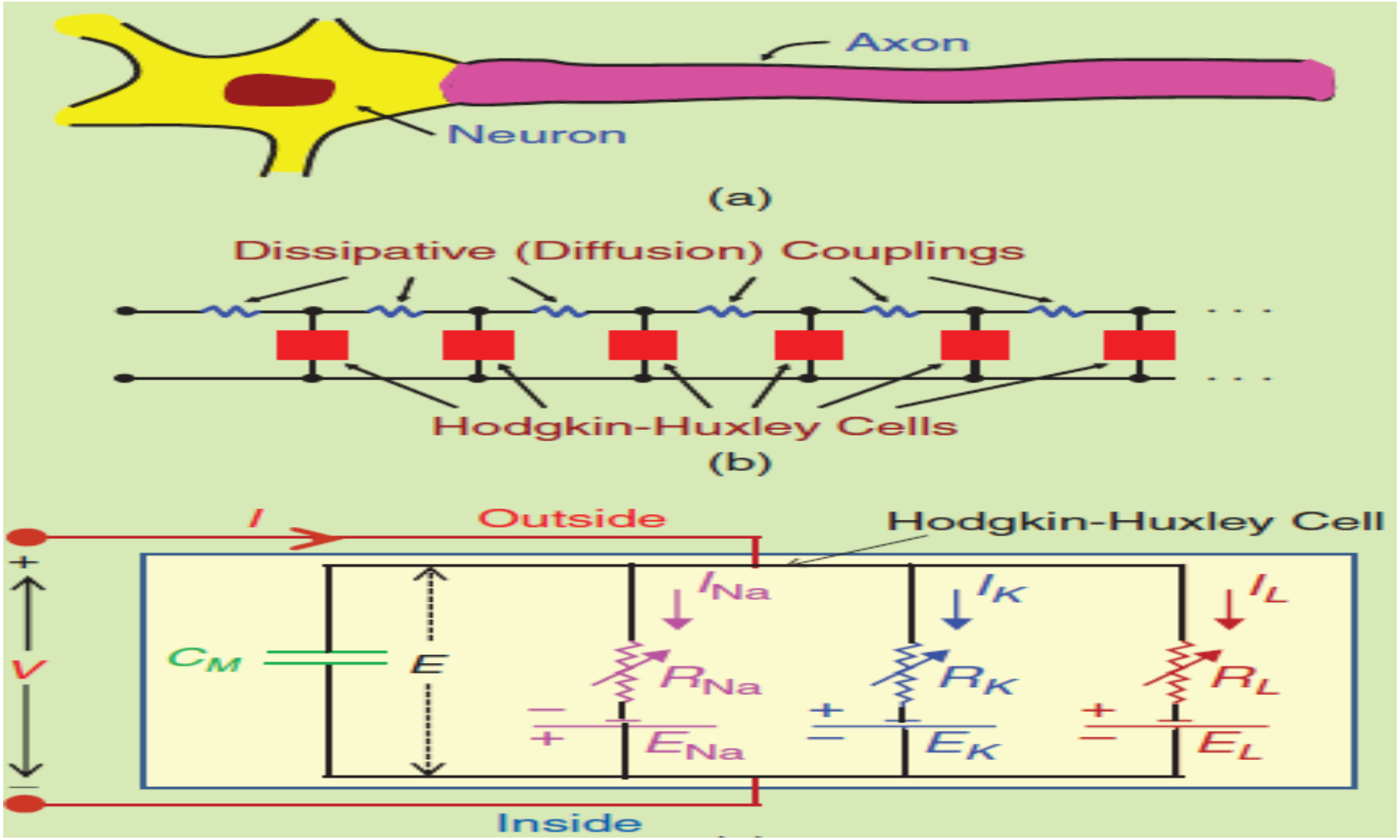
FIG. 1 (color online). Schematic diagrams of the samples grown for these experiments. (i) Reference $LaAlO_3/SrTiO_3$ (substrate); (ii) L layers of homoepitaxial $SrTiO_3$ grown between the substrate and the $LaAlO_3$ cap; (iii) M layers of Mn-doped $SrTiO_3$ grown between the substrate and the $LaAlO_3$ cap; (iv) $N(= L + M)$ layers grown on the $SrTiO_3$ substrate so that the LAO/STO interface is formed between $LaAlO_3$ and undoped homoepitaxial $SrTiO_3$.



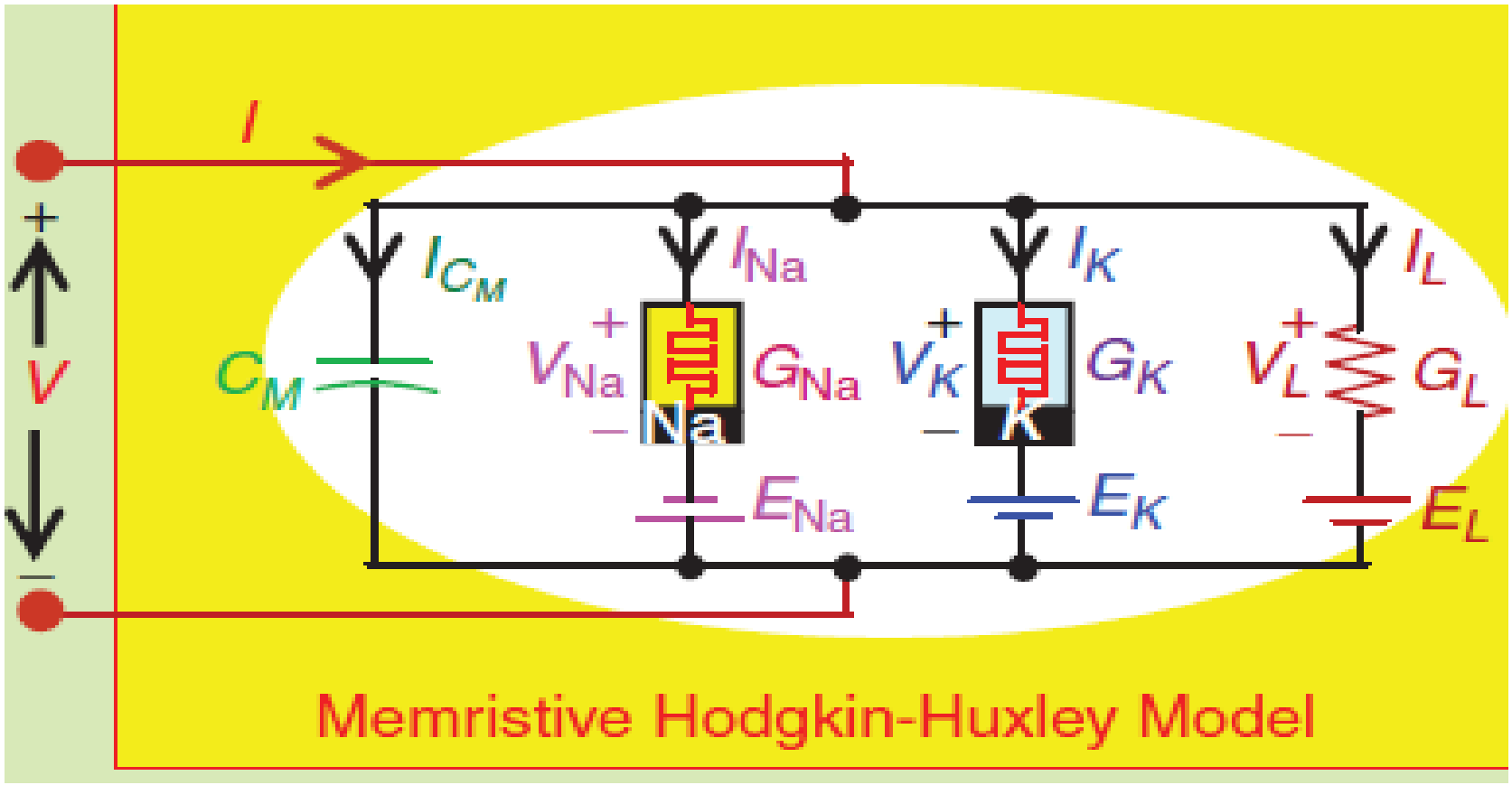
Brains Are Made of Memristors



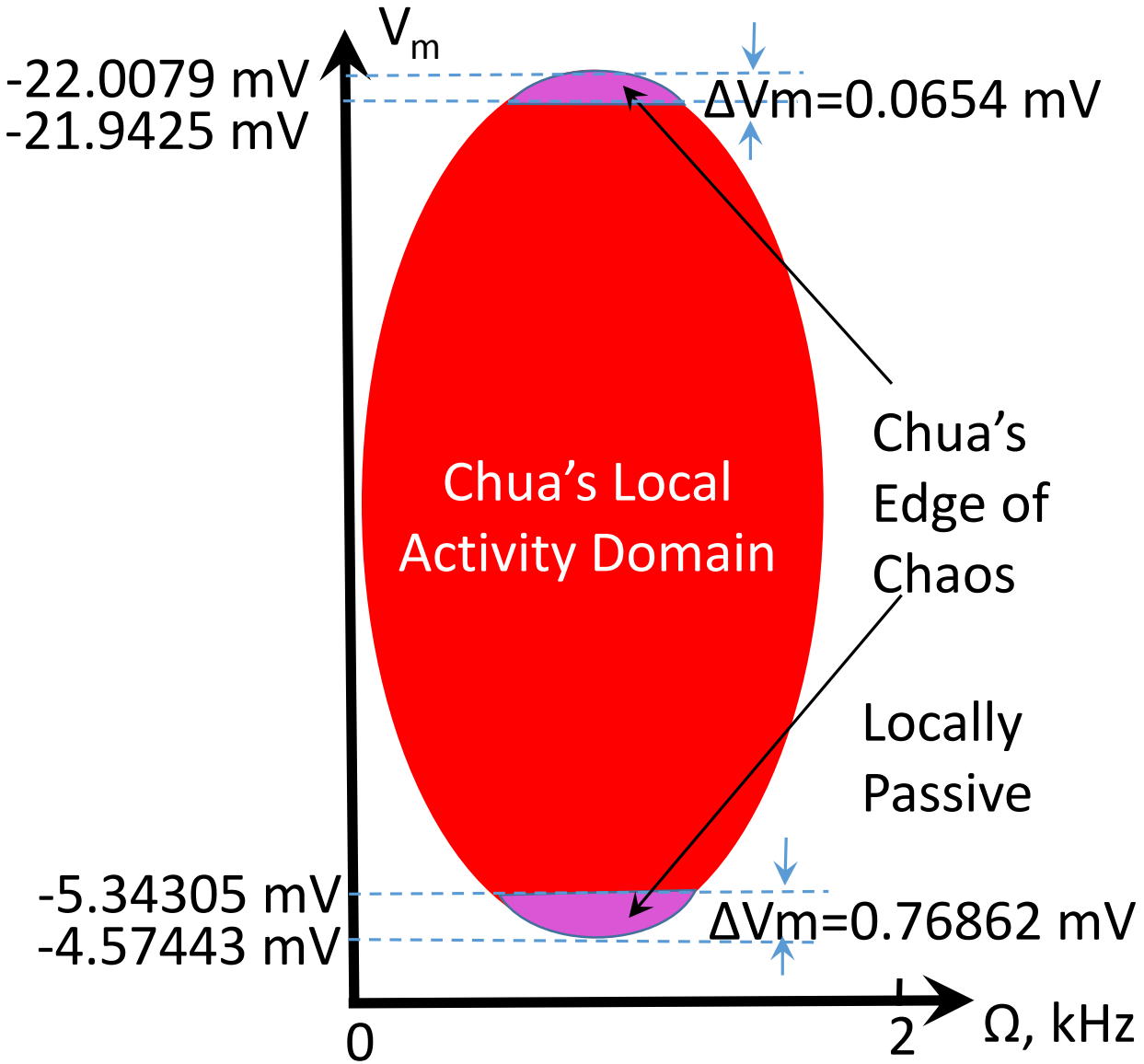
Maheshwar Pd. Sah,
Hyongsuk Kim, and
Leon O. Chua

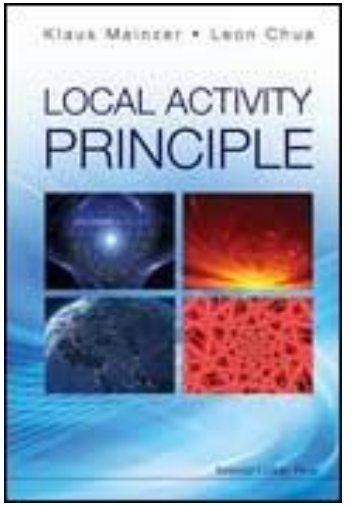


Hodgkin & Huxley described the model in 1952 to explain the mechanisms underlying the initiation and propagation of action potentials in the squid giant axon. They received the 1963 Nobel Prize in Physiology or Medicine for this work.

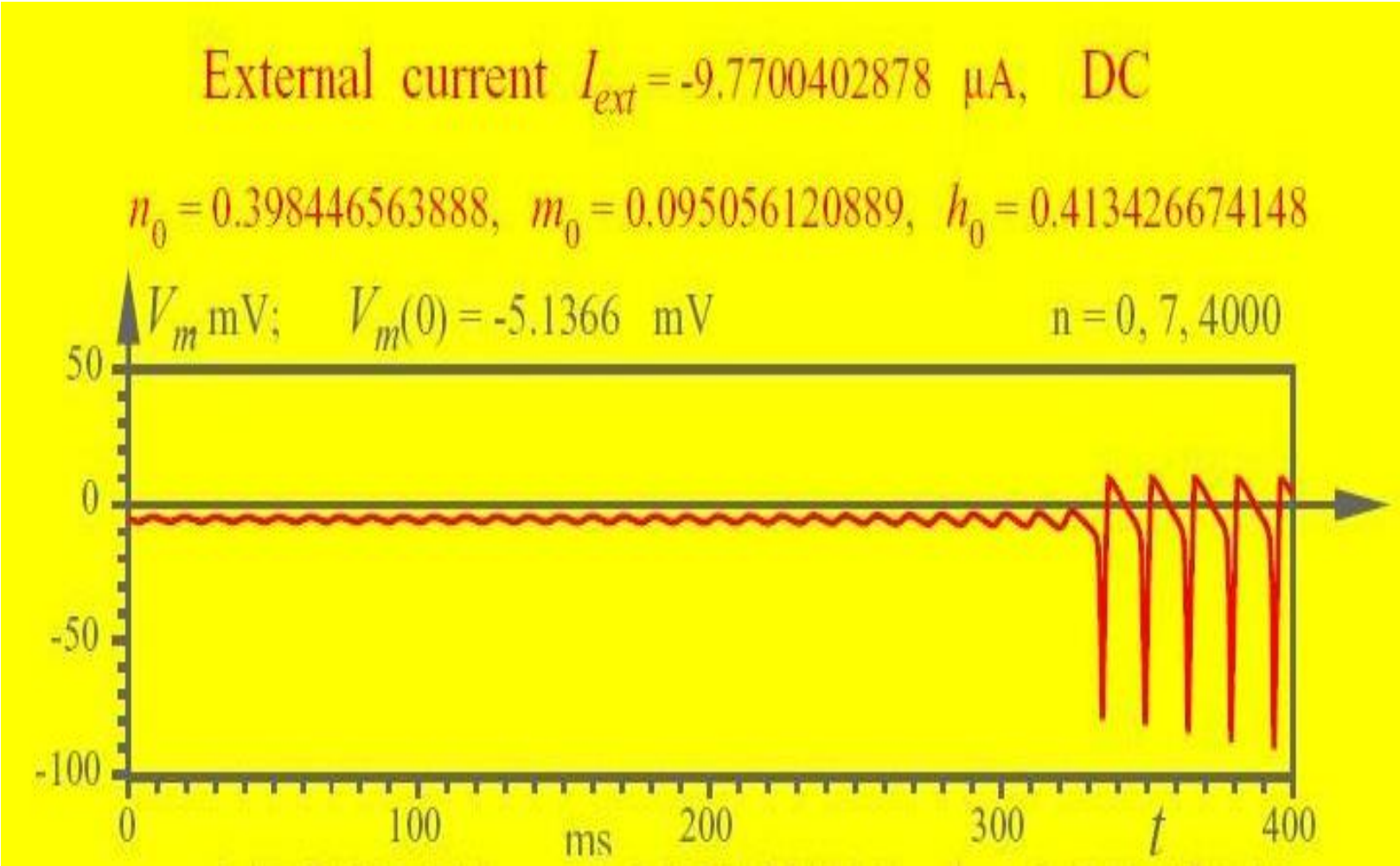


Chua's memristive HH axon circuit model is made of a capacitor, a resistor, three batteries and two memristors. The two memristors were approximated as two time-varying resistors by Hodgkin & Huxley. This approximation had led to numerous anomalies and paradoxes for 70 years.





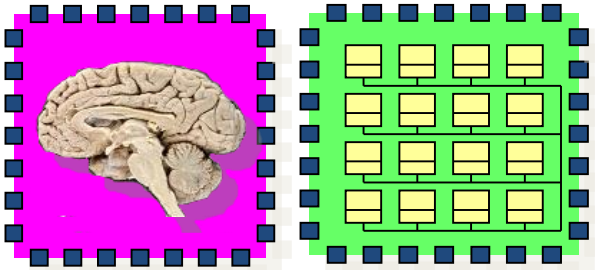
The parameter space. The two disjoint Chua's Edge of Chaos domains (in magenta) are located at the lower and upper tips of the red locally active Islands.



A transient waveform converges to a spike train with the initial condition indicated.

SpiNNaker
Biologically Inspired Massively Parallel Architectures

erc
European Research Council
Established by the European Commission



SpiNNaker (Spiking Neural Network Architecture)

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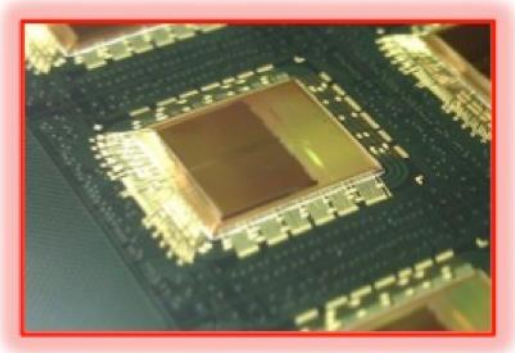
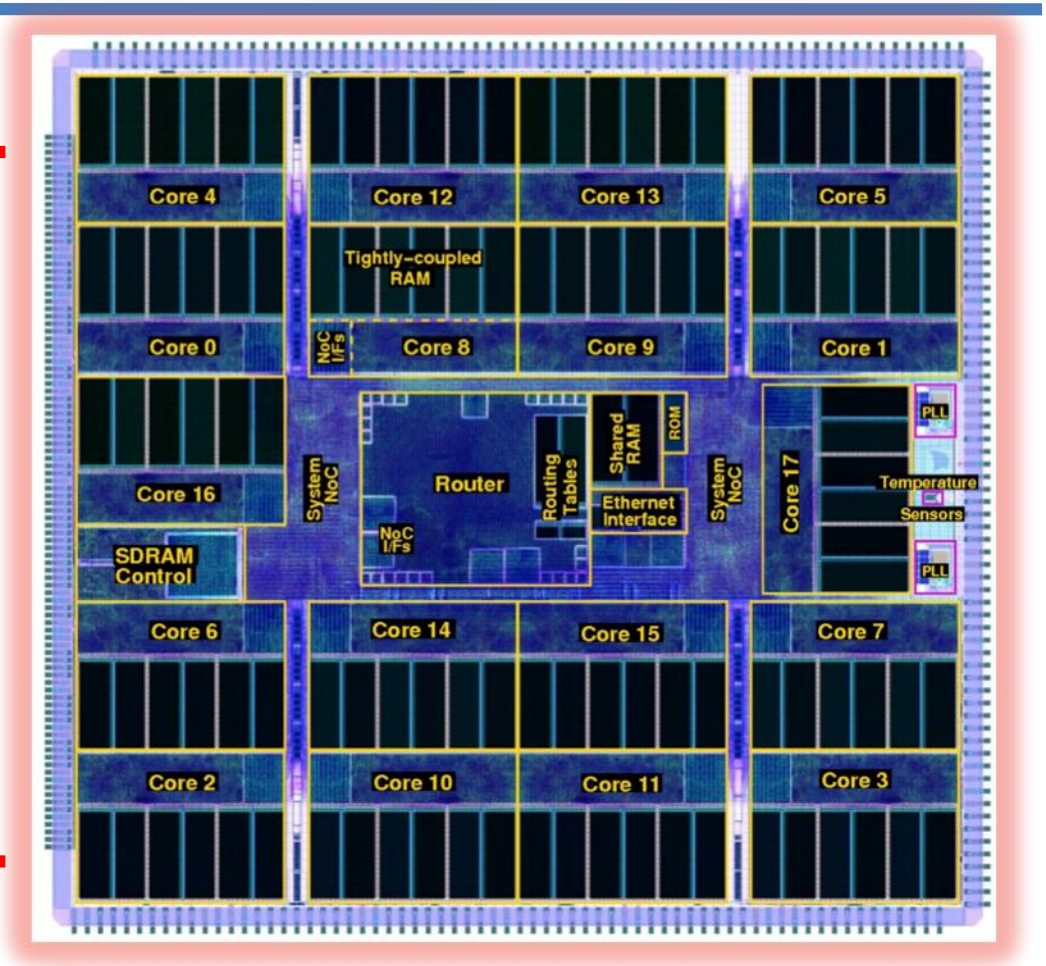
EPSRC University of Cambridge Manchester 1824 The University Of Sheffield. University of Southampton ARM Silistix THALES

SpiNNaker chip



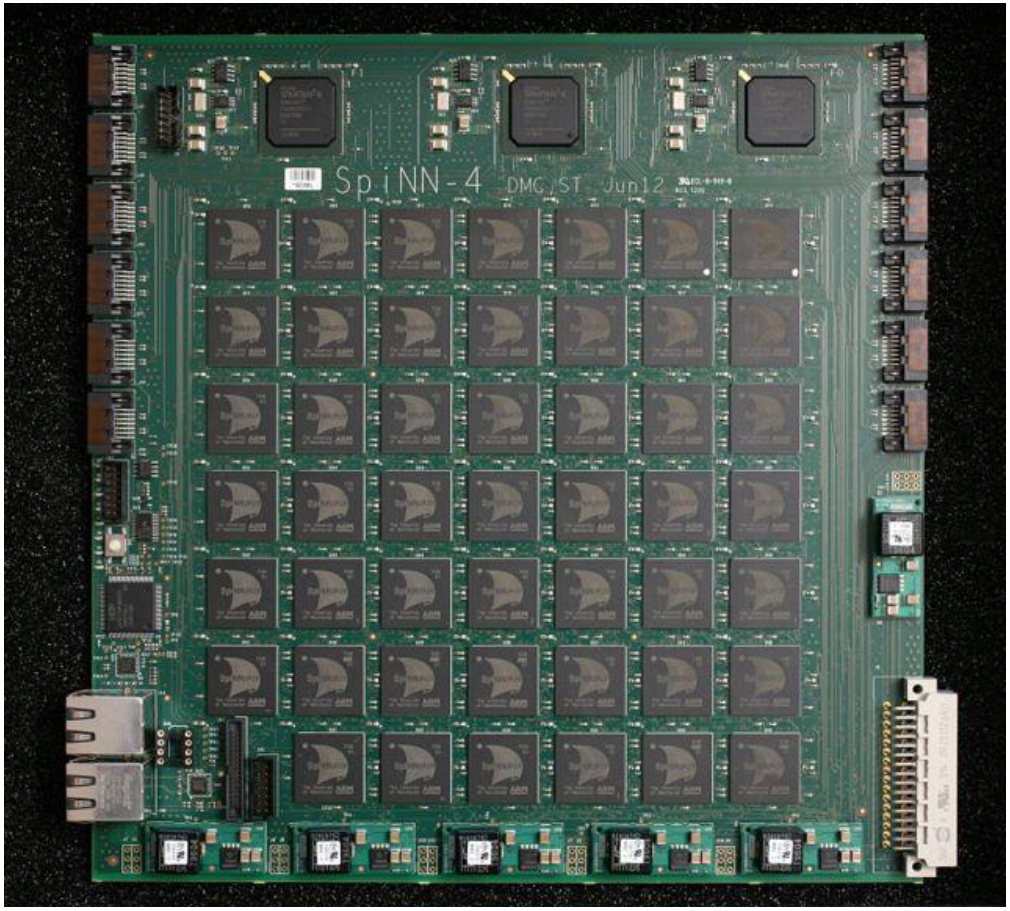
Mobile DDR SDRAM interface

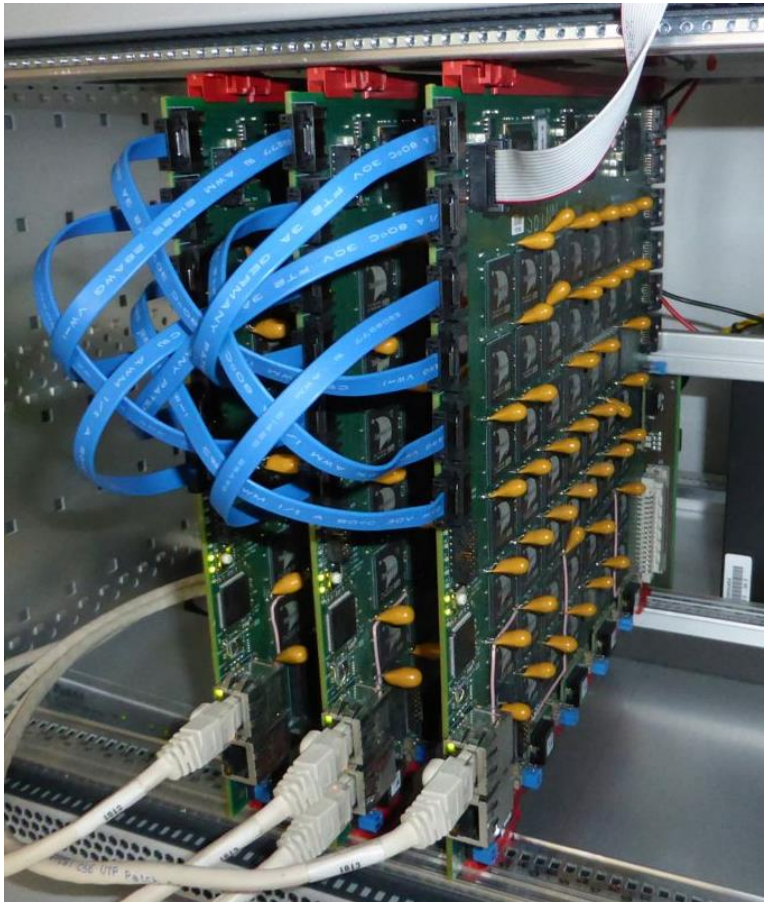
Multi-chip packaging by UNISEM Europe



SpiNNaker
Biologically Inspired Massively Parallel Architectures

48-node PCB





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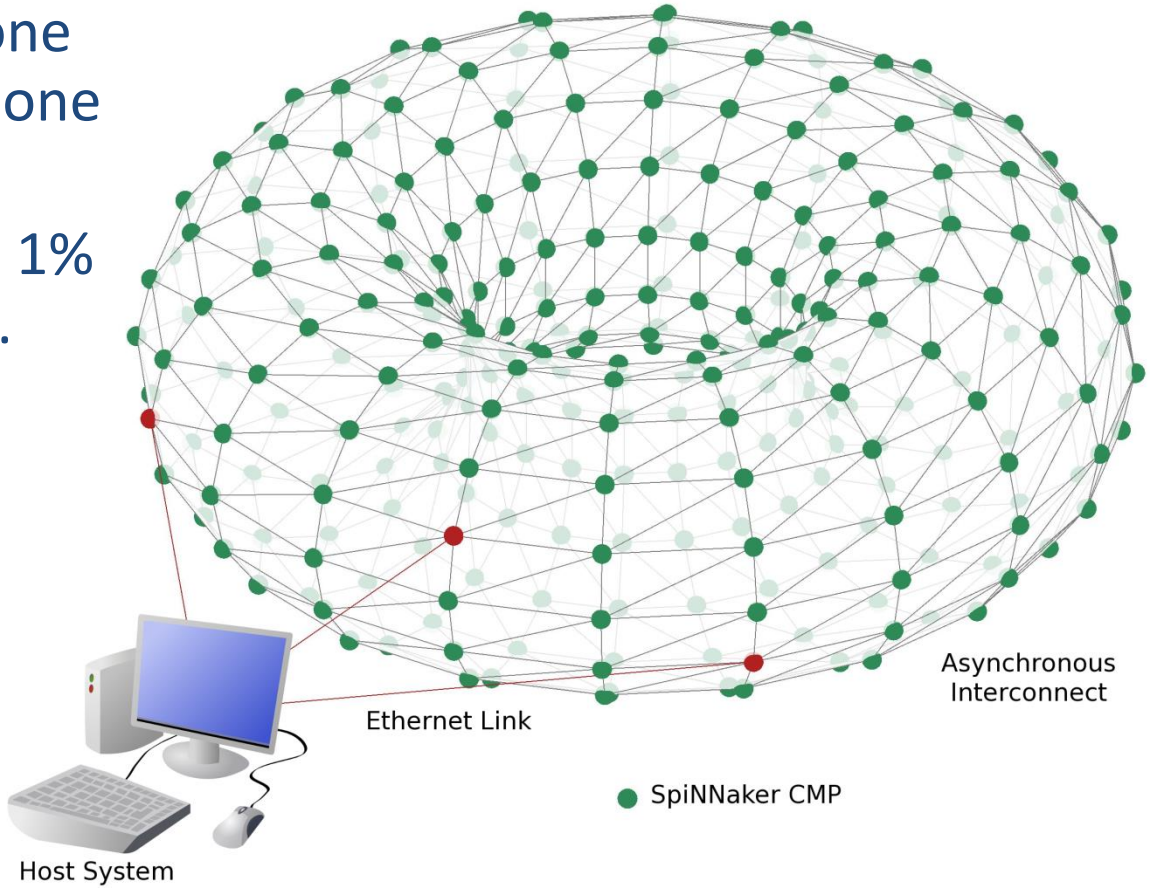
SpiNNaker project

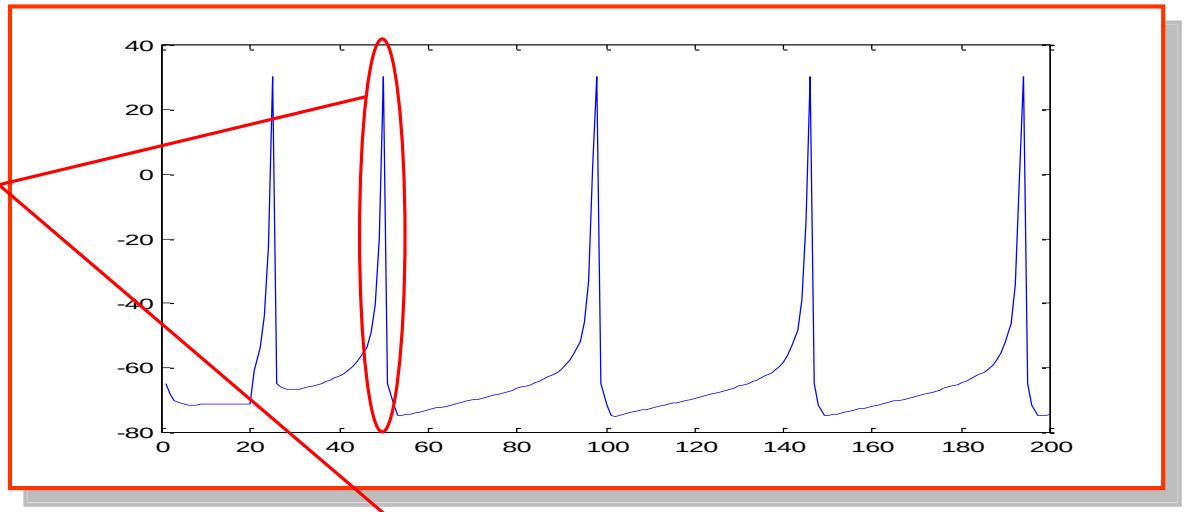
- A million mobile phone processors (ARM) in one computer
- Able to model about 1% of the human brain…
- …or 10 mice!



Communication

- neurons communicate via ‘spike’
- Packet: which neuron fires, and, when it fires
- Timestamp

Packet



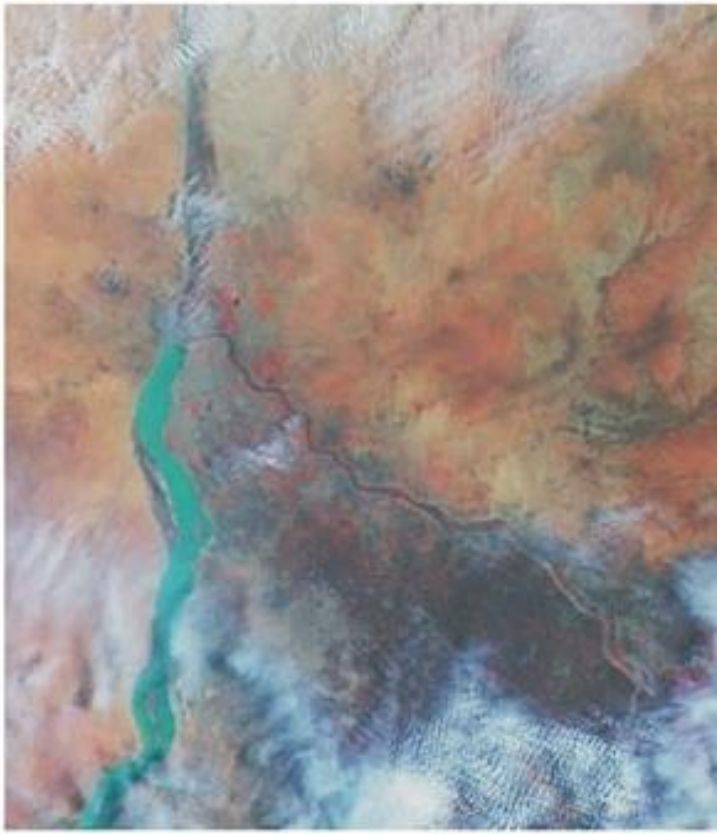
Source (32 bits)

Node (16 bits)	Core (5 bits)	Neuron (11 bits)	Control byte (8 bits)	Payload (32 bits)

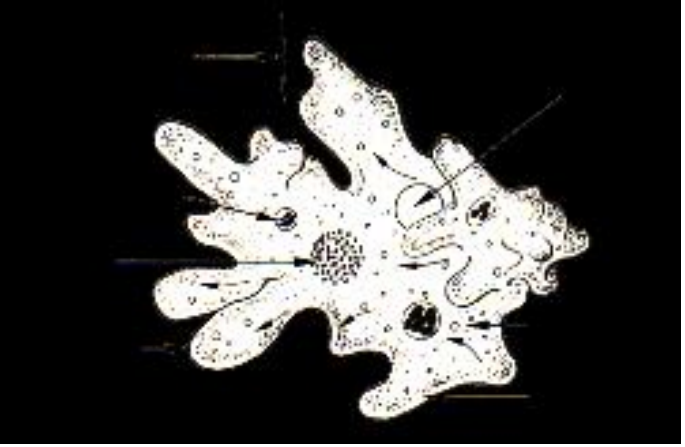
Conclusions

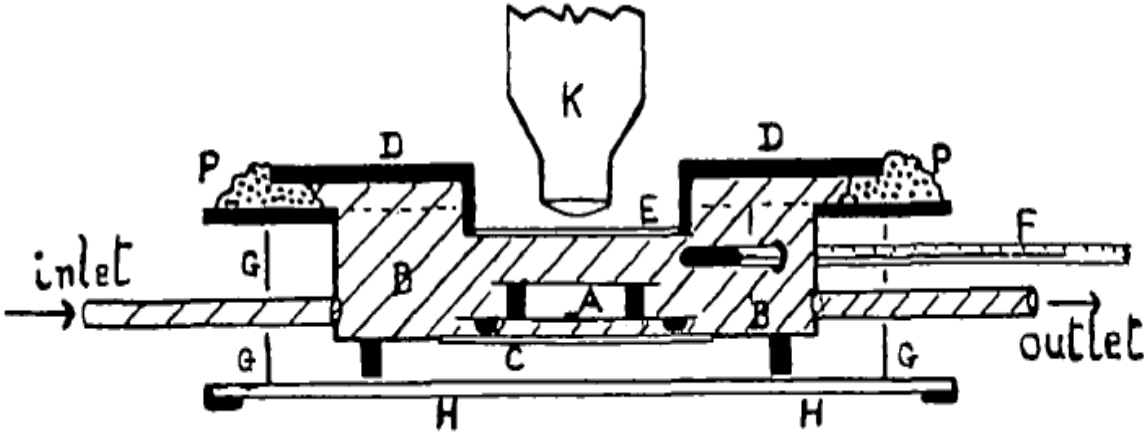
- SpiNNaker has over 1 million cores, 1k simulated neurons per core.
- Capable of simulating very complex networks of 1 billion neurons.
- Interrupt-driven without any operating system running on the cores and central synchronising clock.
- An interrupt arrives (usually in the form of a spike packet); the core wakes up to handle it, possibly emitting more packets of its own as a consequence; and then returns to sleep.
- When a neuron is firing a spike, the time of the spike and the identity of the neuron that emitted the spike need to be conveyed, which is implemented by using packet switched communication and multicast routing.

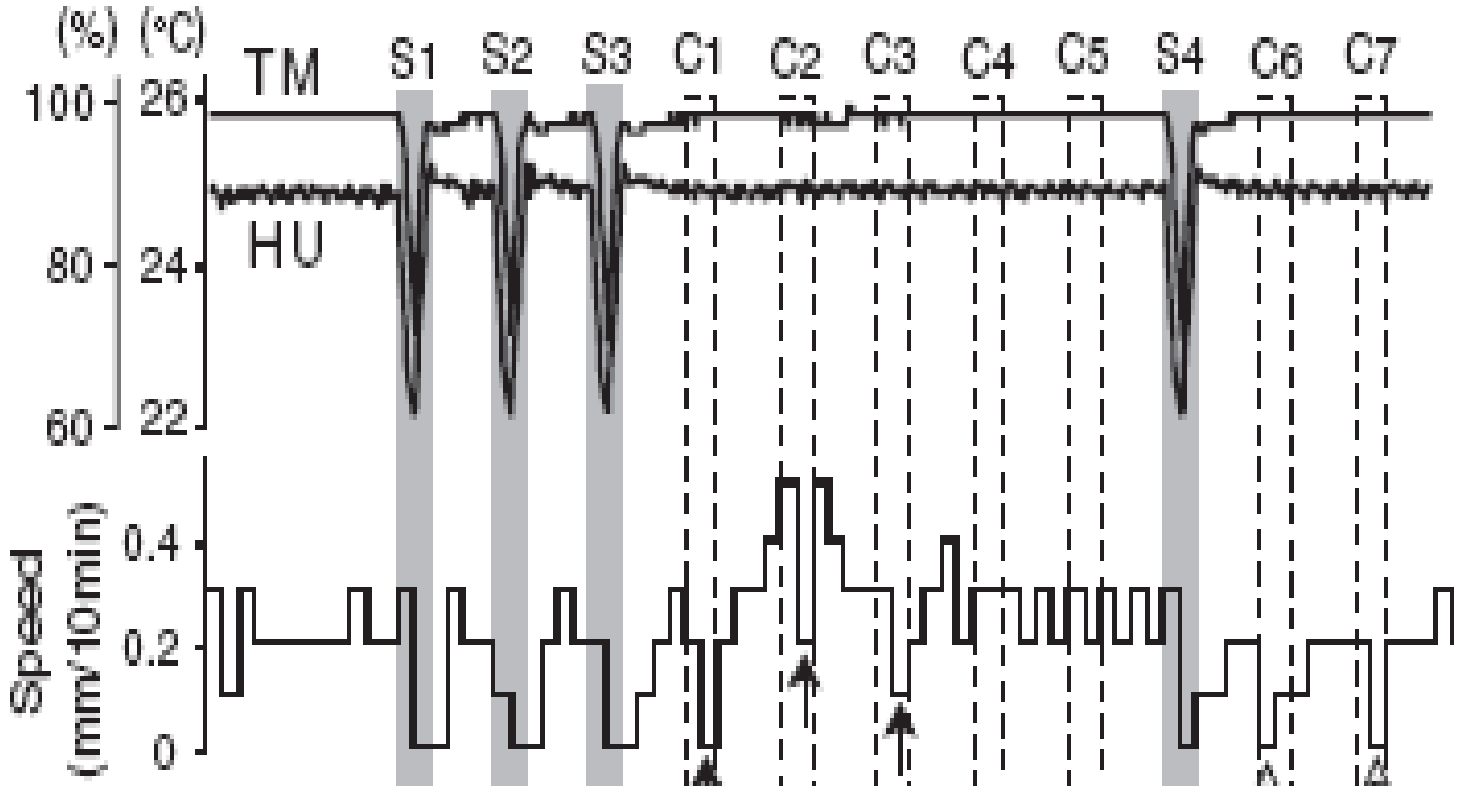
May 1, 2001



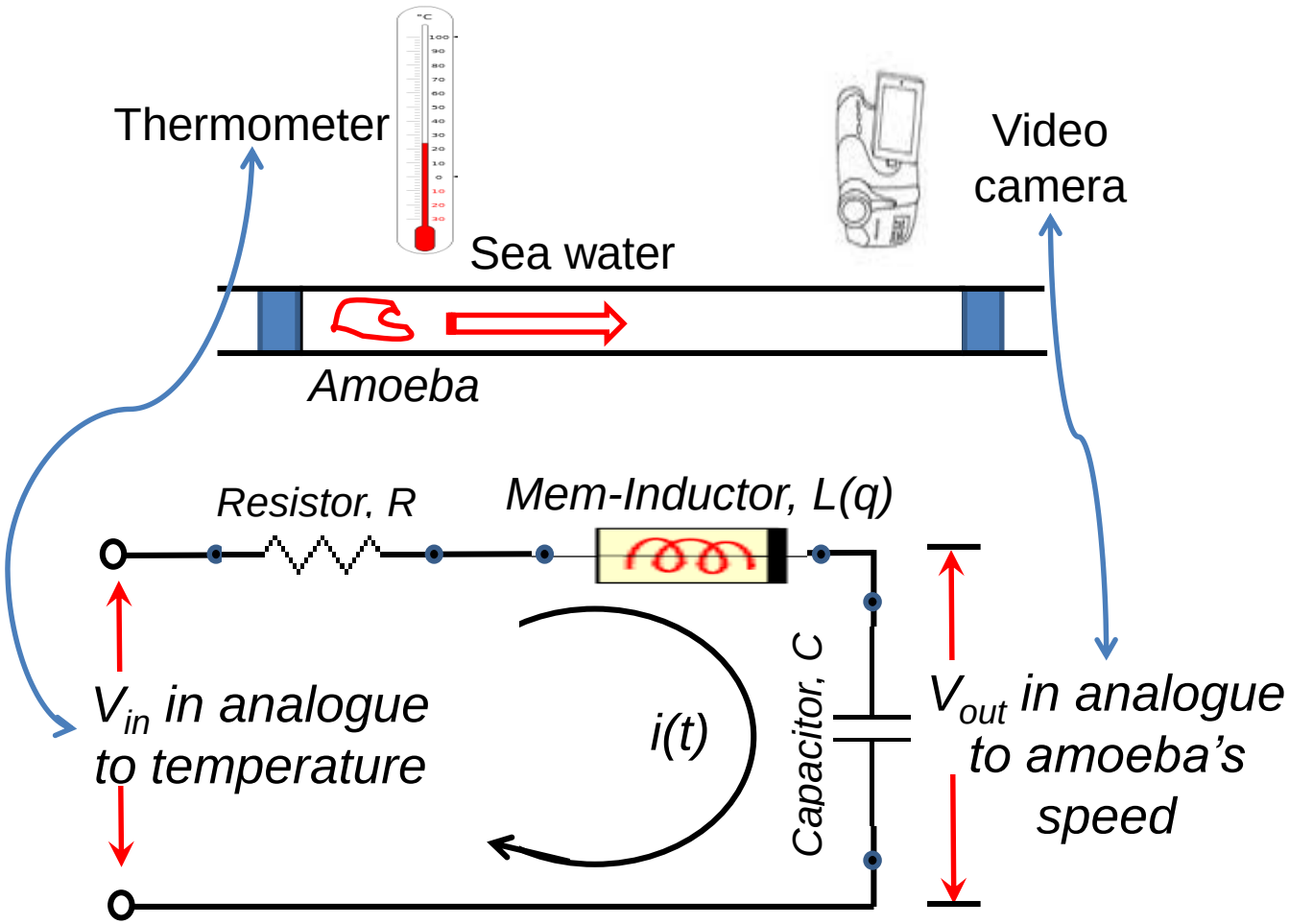
August 21, 2001

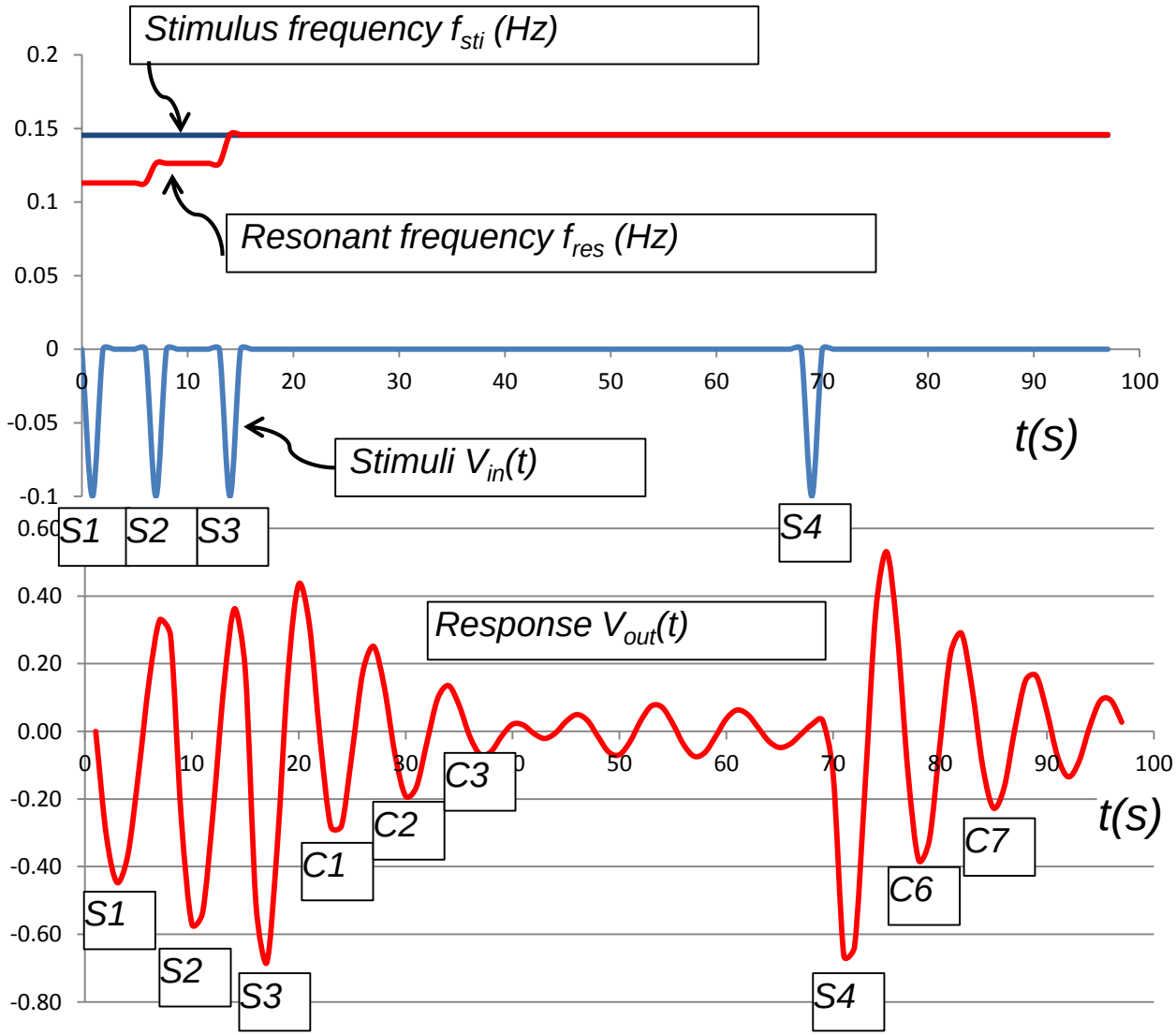


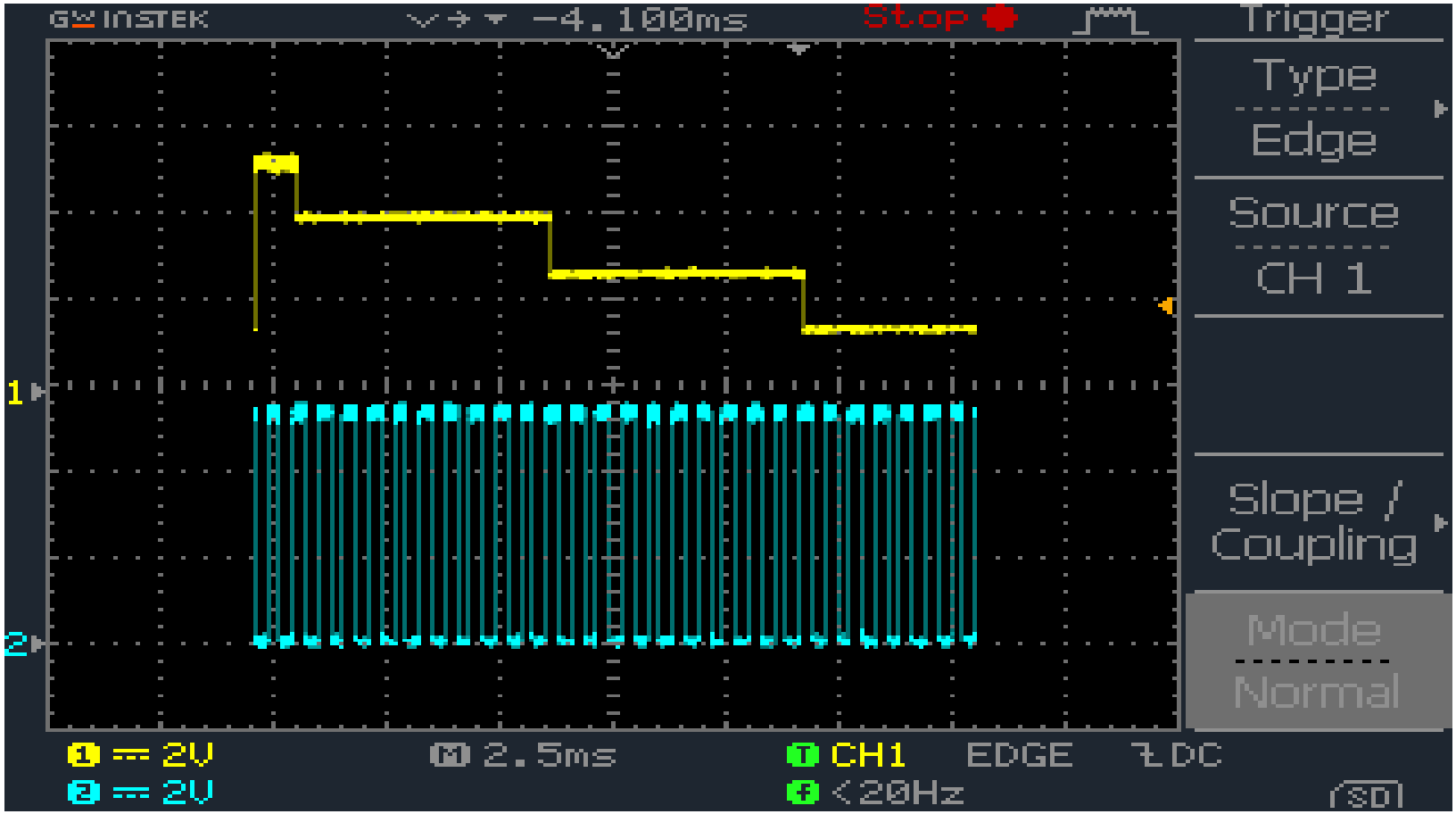




Saigusa, T., Tero, A., Nakagaki, T. & Kuramoto, Y. Amoebae Anticipate Periodic Events. Phys. Rev. Lett. 100, 018101 (2008).


Thermometer
Video camera
Sea water
Amoeba
Resistor, R
Mem-Inductor, L(q)
V_{in} in analogue to temperature
i(t)
Capacitor, C
V_{out} in analogue to amoeba's speed


Stimulus frequency f_{sti} (Hz)
Resonant frequency f_{res} (Hz)
Stimuli $V_{in}(t)$
t(s)
S1
S2
S3
S4
Response $V_{out}(t)$
C1
C2
C3
C6
C7
t(s)


GW INSTEK
-4.100ms
Stop
Trigger
Type
Edge
Source
CH 1
Slope /
Coupling
Mode
Normal
1
2
1 = 2V
2 = 2V
M 2.5ms
T CH1 EDGE DC
<20Hz

NN: 3155 Model 5G pp. 1–6 (col. fig: NIL)

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Neural Networks xx (xxxx) xxx–xxx

Contents lists available at SciVerse ScienceDirect

Neural Networks

journal homepage: www.elsevier.com/locate/neunet

2013 Special Issue

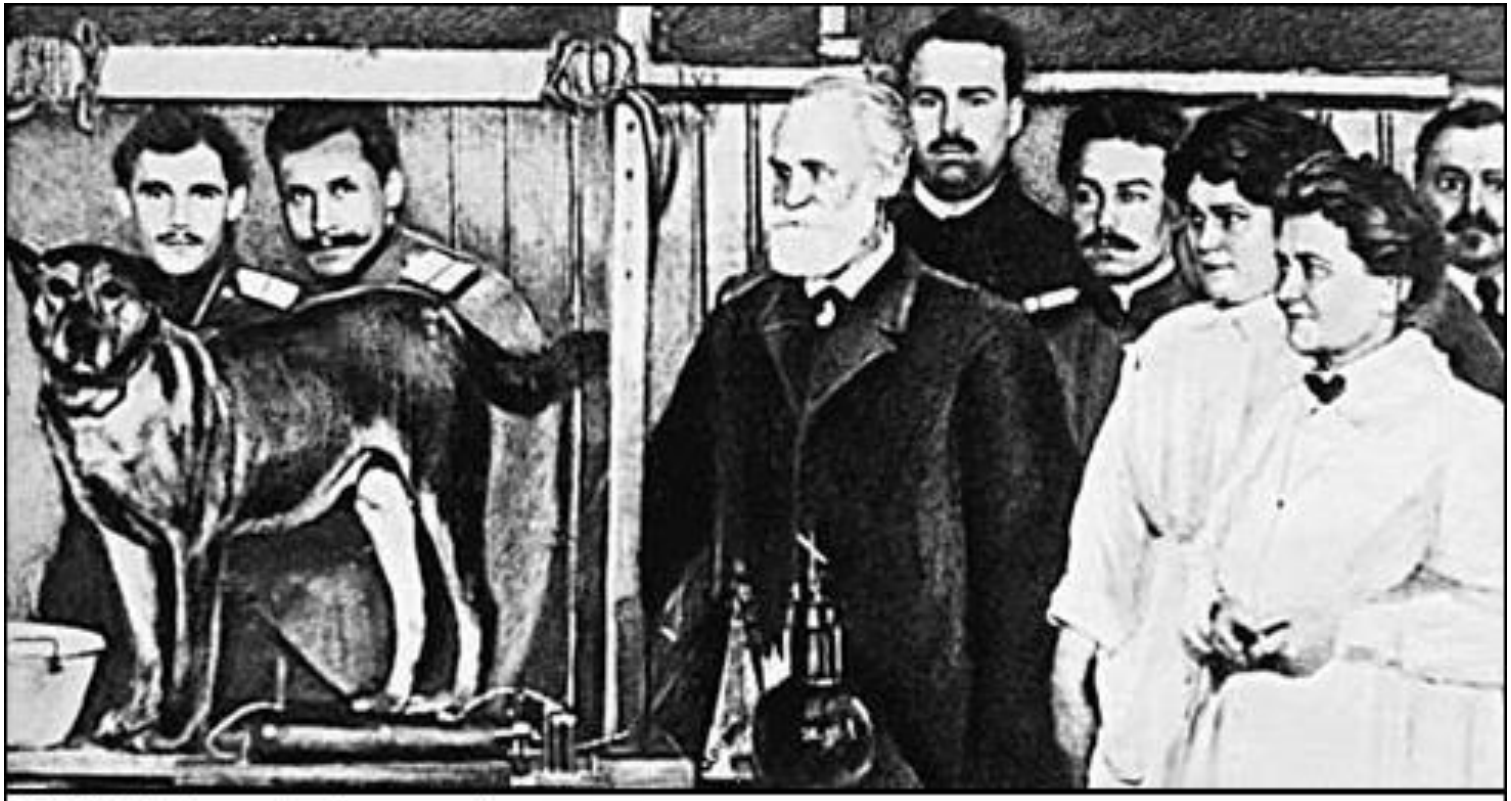
Adaptive Neuromorphic Architecture (ANA)

Q1 Frank Zhigang Wang[a,*], Leon O. Chua[a,b], Xiao Yang[a], Na Helian[c], Ronald Tetzlaff[d], Torsten Schmidt[d], Caroline Li[a], Jose Manuel Garcia Carrasco[e], Wanlong Chen[a], Dominique Chu[a]

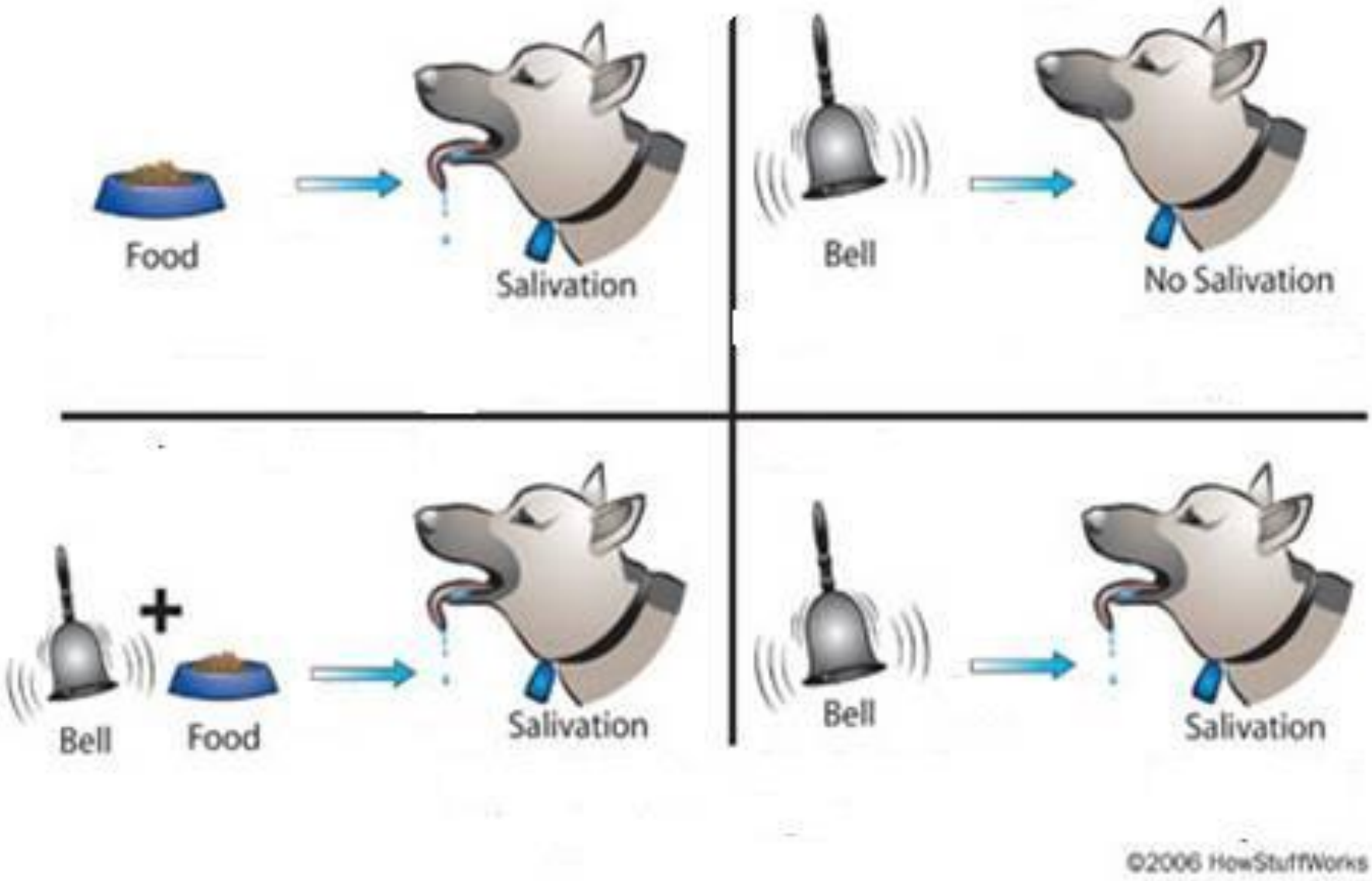
[a] School of Computing, University of Kent, UK

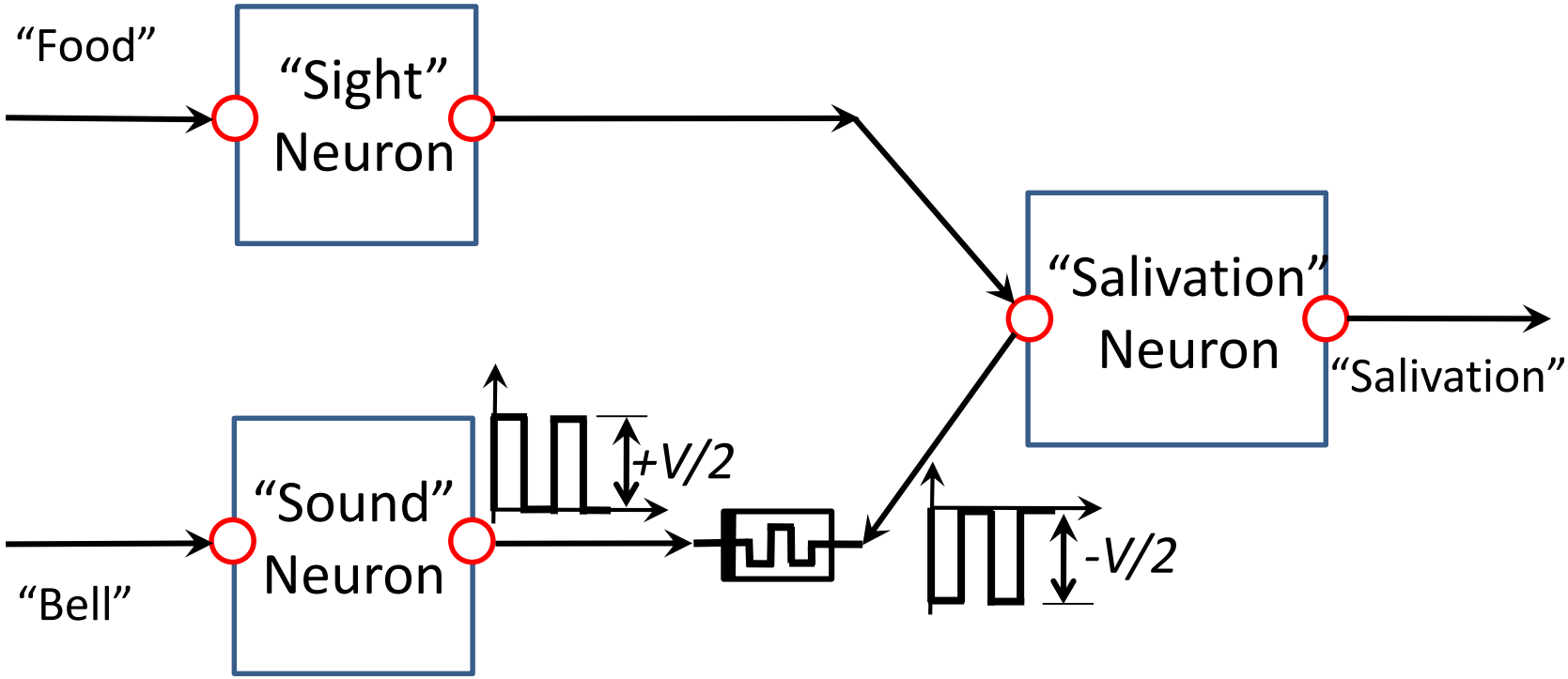
[b] Department of Electrical Engineering and Computer Science, University of California, Berkeley, USA

Pavlov's Dog



© 1997 The Learning Company, Inc.

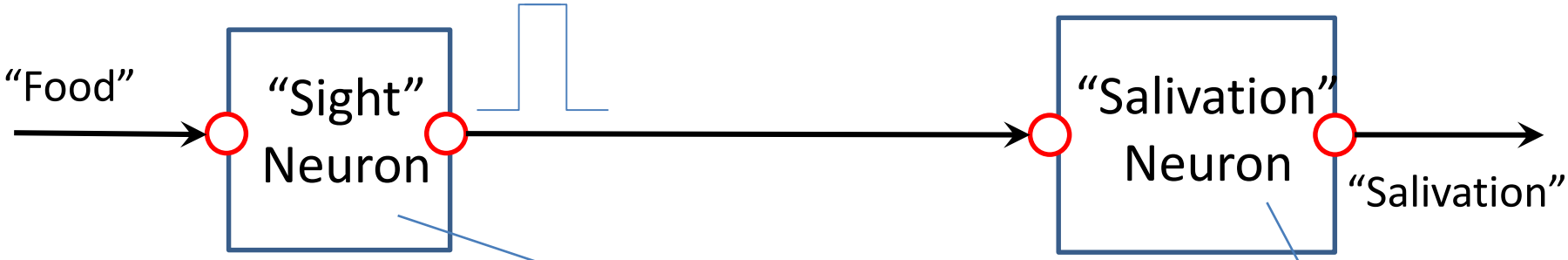


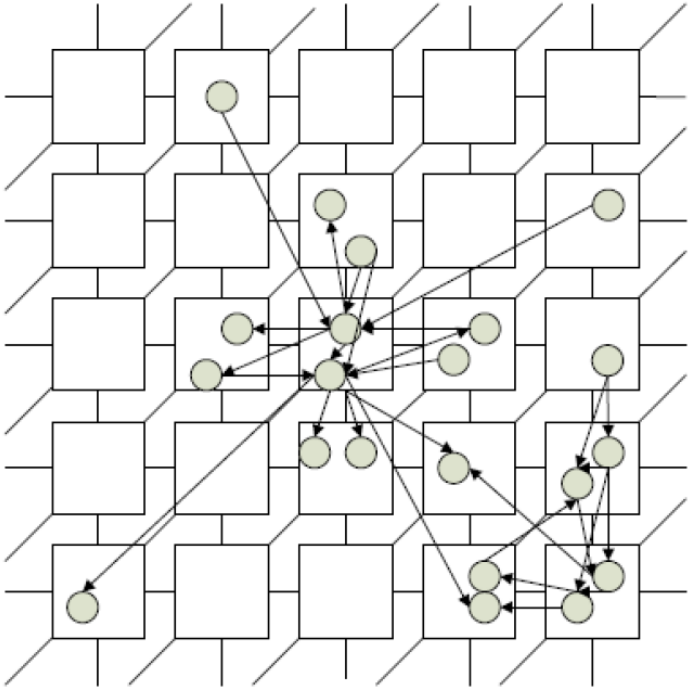


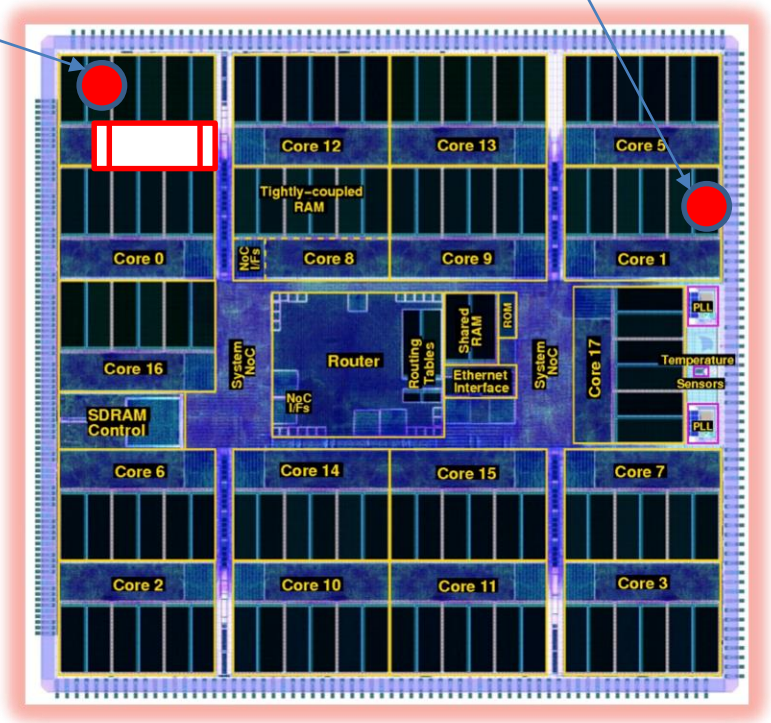
Hebbian rule

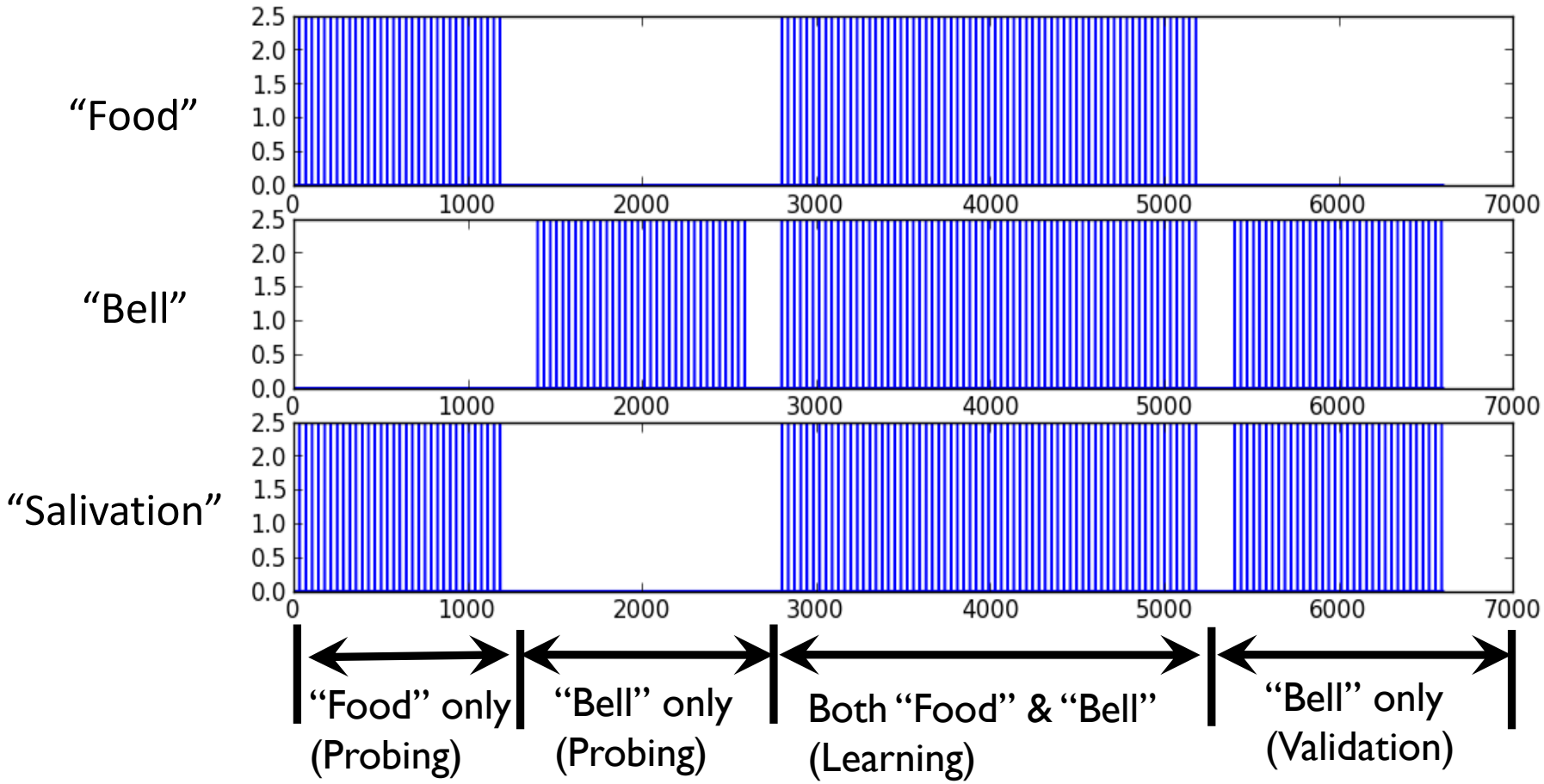
"neurons that fire together, wire together"

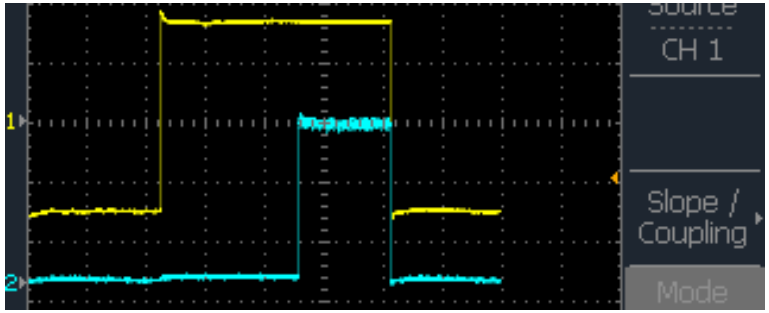
In Spinnaker …



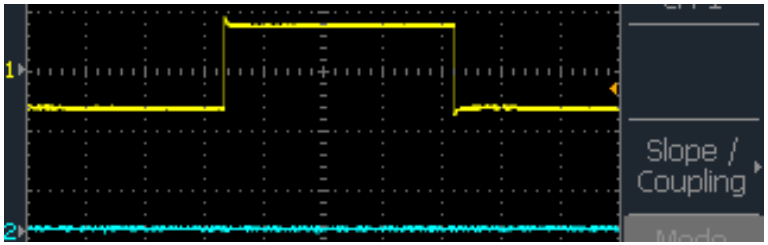




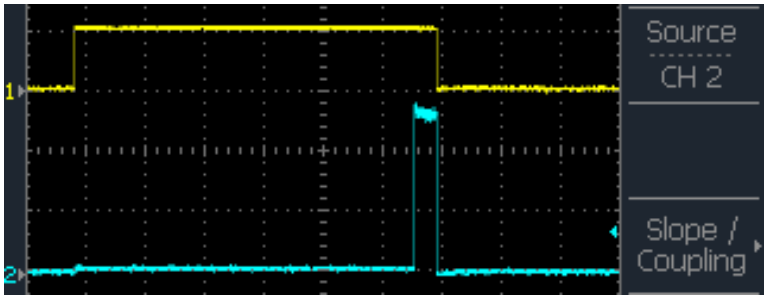

"Food"
"Bell"
"Salivation"
2.5
2.0
1.5
1.0
0.5
0.0
0
1000
2000
3000
4000
5000
6000
7000
"Food" only
(Probing)
"Bell" only
(Probing)
Both "Food" & "Bell"
(Learning)
"Bell" only
(Validation)



(a) A “Full Voltage” causes a delayed switching;



(b) A “Half Voltage” causes no switching;



(c) A long “Half Voltage” still causes an unwanted switching.

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Delayed switching applied to memristor neural networks

Frank Z. Wang,[1,a)] Na Helian,[2] Yike Guo,[3] Sining Wu,[1] Xiao Yang,[1] Guan Lim,[1] and Md Mamunur Rashid[4]

[1]*Future Computing Group, School of Computing, University of Kent, United Kingdom*
[2]*School of Computer Science, University of Hertfordshire, United Kingdom*
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[4]*CERN, Geneva, Switzerland*

(Presented 3 November 2011; received 28 September 2011; accepted 26 October 2011; published online xx xx xxxx)

Magnetic flux and electric charge are linked in a memristor. We reported recently that a memristor has a peculiar effect in which the switching takes place with a time delay because a memristor possesses a certain inertia. This effect was named the "delayed switching effect." In this work, we elaborate on the importance of delayed switching in a brain-like computer using memristor neural networks. The effect is used to control the switching of a memristor synapse between two neurons

1. Memristor-based Brain-like Computer
2. Green Computing
3. Cloud Computing/Big Data

Why Green?

- 40-50% of corporate energy consumption goes to IT
- Computing-centre power costs have doubled in five years
- Energy costs will exceed hardware costs
- Regulations are being introduced in EU & US

UNIVERSITY OF CAMBRIDGE

Cranfield UNIVERSITY

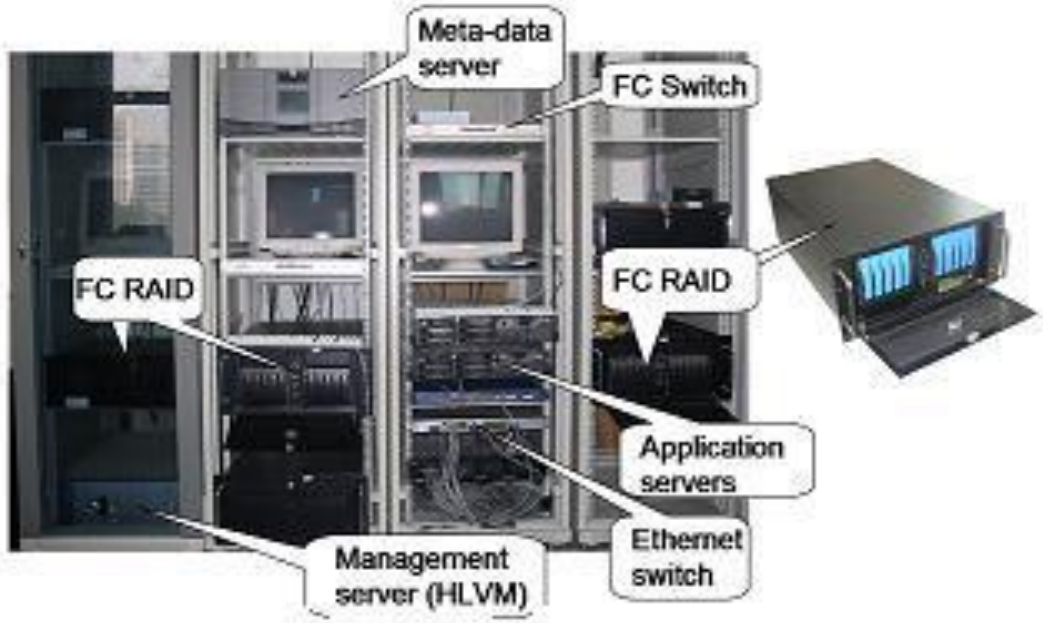
Research

Cambridge-Cranfield HPCF > Research

Centre for Grid Computing

The advent of the computational grid b
It would change dramatically human ca
implications. Sooner or later, everybo
that we were by the Internet. Grid Com
production. In 2001, Forbes predicted the grid would be
year 2020. The Centre for Grid Computing (CGC) is do
Mining and Data-Intensive Computing on the Grid platfo
For more details see the Centre for Grid Computing Ho

400,000 GBP/yr to cover water & electricity bills



Sunfire Galaxy-class supercomputer at Cambridge-Cranfield HPCF listed as the 343rd in Top500 Super Computers in the world.

Disk

=

Disk

+

Flash (DiskOnModule, DOM)

=

Hybrid Disk

--- Frank Wang, et al., “Redundant Array of Hybrid Disks (RAHD)”, IEEE Transactions

1. Memristor-based Brain-like Computer
2. Green Computing
3. Cloud Computing/Big Data

THE IEEE 3RD INTERNATIONAL CONGRESS ON BIG DATA (BIGDATA 2014), ALASKA, USA, JUNE 27-JULY 2, 2014

CloudJet4BigData: Streamlining Big Data via an accelerated socket interface

Frank Zhigang Wang	Theo Dimitrakos	Na Helian	Sining Wu	Ling Li	Rodric Yates
School of Computing	British Telecommu-	SCS	Xyratex	SoC	Hursley Lab.
University of Kent	nication	University of	Havant	University of Kent	IBM
UK	UK	Hertfordshire	UK	UK	UK

IEEE TRANSACTIONS ON COMPUTERS, VOL. 56, NO. 4, APRIL 2007

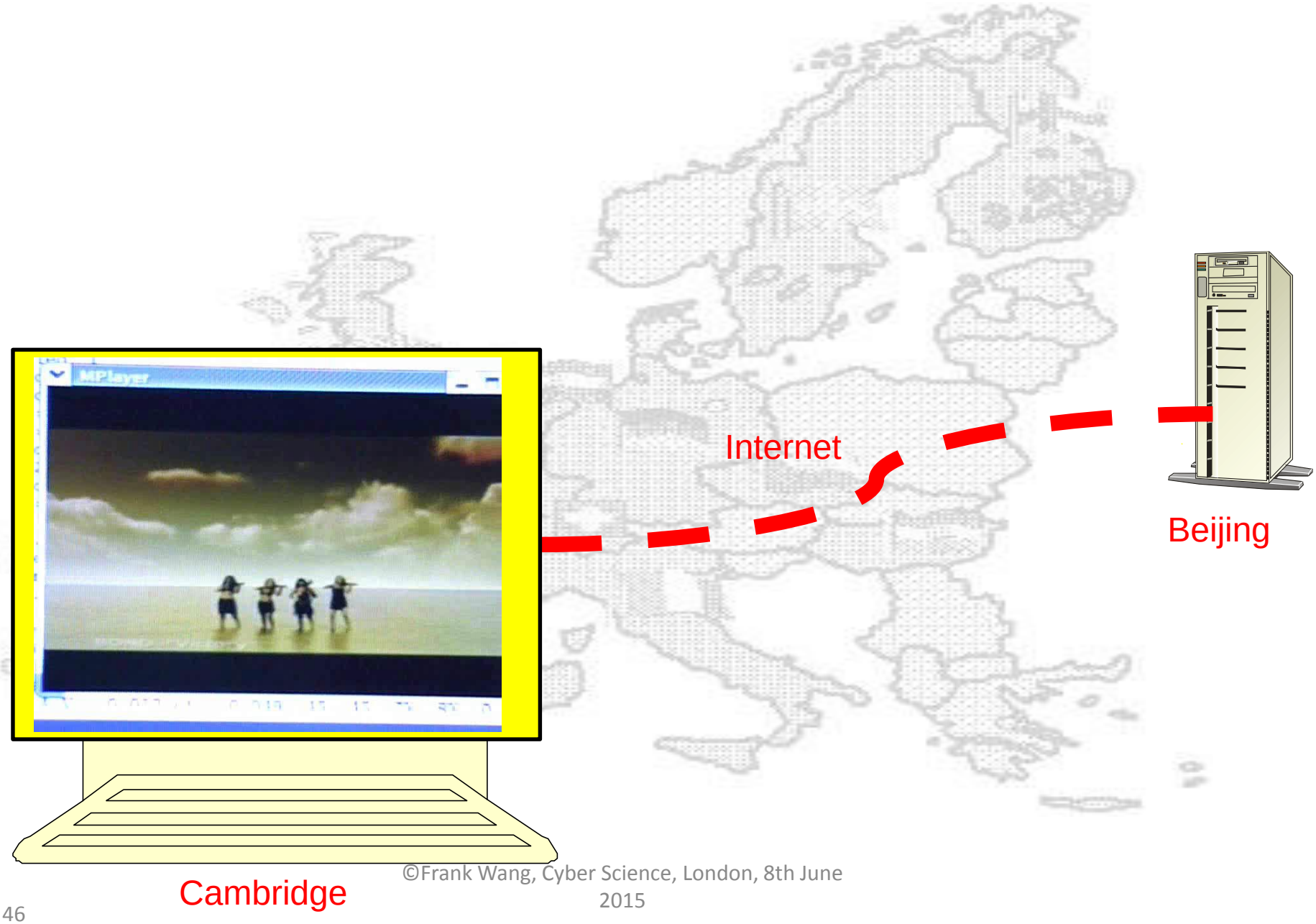
Grid-Oriented Storage: A Single-Image, Cross-Domain, High-Bandwidth Architecture

Frank Zhigang Wang, *Senior Member, IEEE*, Sining Wu, Na Helian, Michael Andrew Parker, Yike Guo, Yuhui Deng, and Vineet R. Khare

ACM Operating Systems Review

A Heterogeneous Storage Grid Enabled by Grid Service

Yuhui Deng, Frank Wang
Center for Grid Computing, Cambridge-Cranfield High Performance Computing Facilities,
Cranfield University Campus, Bedfordshire MK43 0AL, United Kingdom
y.deng@cranfield.ac.uk, f.wang@cranfield.ac.uk




CloudJet on
EuroAsiaGrid
Beijing
Cambridge

Comments from independent reviewers:

- This proposed work has all the potentials of keeping the UK research and development – world class.
- It is certainly first of its kind.

Finalist Award

ACM/IEEE
Super Computing

Finalist Project: Grid-oriented Storage: Parallel Streaming Data Access to Accelerate Distributed Bioinformatics Data Mining

Finalist team: Frank Z. Wang (Centre for Grid Computing, Cambridge-Cranfield HPCF),, Sining Wu, Yuhui Deng, Vineet R. Khare & Chenhan Liao (Centre for Grid Computing, Cambridge-Cranfield HPCF), Amir Nathoo; Rodric Yates; Paul Fairbairn (IBM Hursley Laboratory), Jon Crowcroft, Jean Bacon, Michael Andrew Parker (Cambridge University), Zhiwei Xu (Institute of Computer Technology), Yike Guo (Imperial College)

Grants…

- EC FP7 Grant (300k euros) “Re-discover Basic Circuit Element Table”
- EPSRC/DTI grant (1 million GBP) “Grid-oriented Storage: Next Generation Architecture”
- EPSRC grant (470k GBP) "Accelerating NFS/CIFS over the WAN/Grid“
- EC FP7 Grant (1.01 million euros) “QuickLinux”
- EC FP6 Grant (400k euros) “EuroAsiaGrid”
- ……

An Evolutionary History of Computer Science

1822 Charles Babbage
1937 Iowa State University
1939 Alan Turing
1943 ENIAC
1953 COBOL
1958 Integrated circuit
1964 Mouse/GUI
1971 Floppy disk
1971 Memristor by Leon Chua
1973 Ethernet
1974 IBM PC
1976 Apple
1985 MS Windows
1990 WWW by Tim Berners-Lee
1999 Wi-Fi
2004 Firefox
2008 HP Memristor
2010 iPad
2012 Memristors: Brain-like computer
2014 SpiNNaker (BCS Lovelace Medal)
2025 Future Computers???

Computing towards 2025

Concepts and technologies developed within computer science are starting to have wide-ranging applications outside the subject (as mathematics in physics).

Computing towards 2025

- Service
- Intelligence
- Connectivity
- Mobility
- Interactivity

Computing towards 2025

- If Moore's law continues to hold true, computers would be 32 times more powerful than the current models.
- Green computing will prove itself to be the most concerning issue as computing becomes increasingly pervasive.
- Computer science will be at the heart of future revolutions in business, science, and society.

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THE QUEEN'S ANNIVERSARY PRIZES